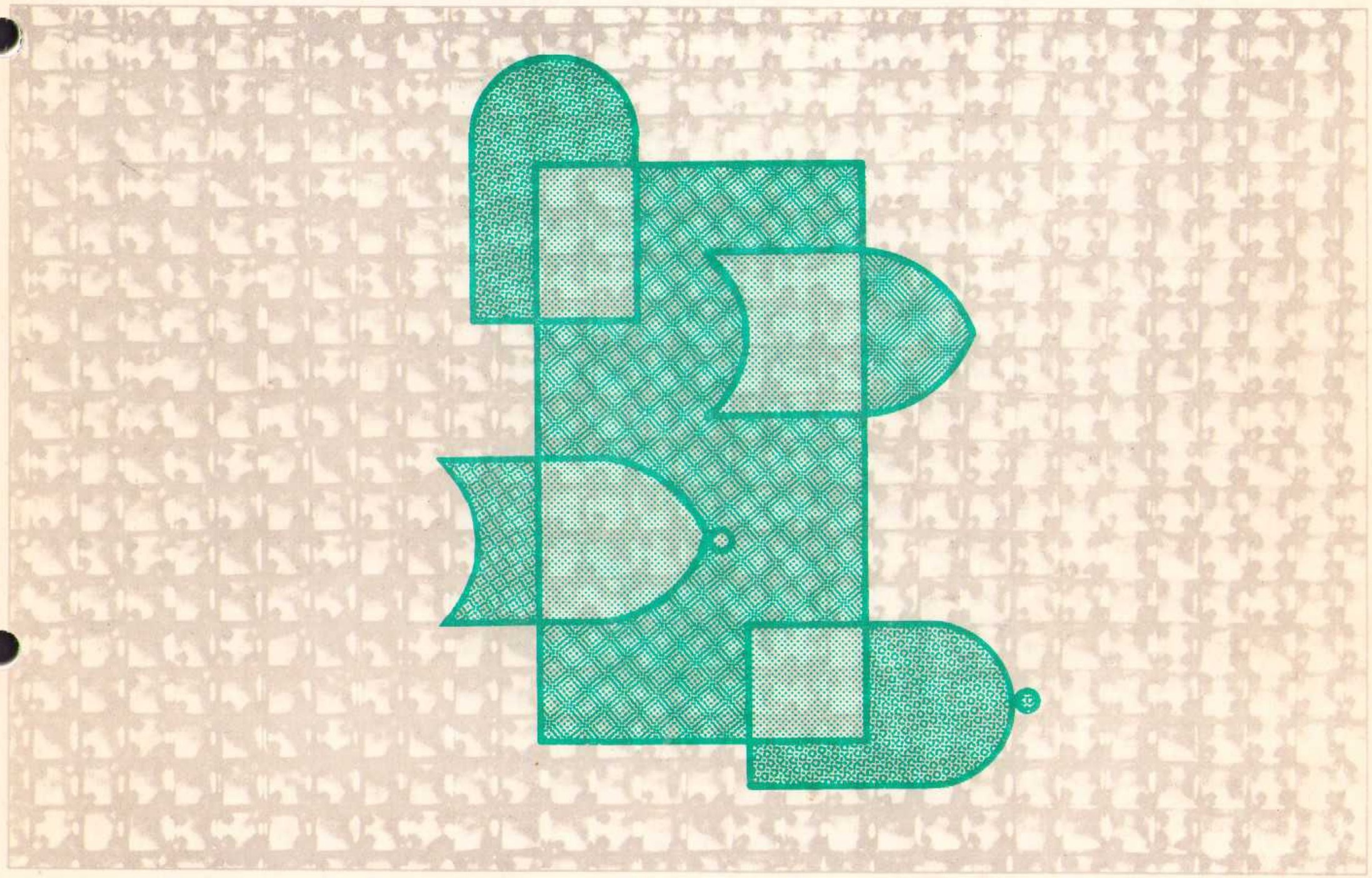
TECHNISCHE DOCUMENTATIE 1970

DEEL 1 2 3 4 5 6 7 8 9 10 (11) (12)

TECHNISCHE GEGEVENS TTL



van oorn
ELEKTRONICA

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Voor de leveringsvoorwaarden, doelstelling, abonnementen, verscheidingsdata, enz. zie technische documentatie 1970 deel 1 t/m 4, pagina 2 en 3.

- -

Inleiding: Coördinatie: Paul E. Annokkee

Deze laatste twee delen van 1970 zijn wederom bij elkaar gevoegd, aangezien één onderwerp wordt behandeld. Uit de door ons ingestelde enquète in deel 10 van de documentatie is gebleken, dat voor de technische gegevens van TTL IC's een ruime belangstelling aanwezig is: op de navolgende 64 pagina's worden de meest belangrijke nieuwe typen behandeld. Ons TTL leveringsprogramma is inmiddels in zijn volledigheid uitgebreid; de typenummers zijn opgenomen op pagina 64 van deze documentatie; van de niet gepubliceerde typen zijn tegen vergoeding de datasheets in de vorm van fotocopieën beschikbaar; de aansluitingen van alle IC's worden echter in onze uitgave van 1971 opgenomen.

De eerste delen van de jaargang 1971 zijn inmiddels in voorbereiding (3 delen in één) en zullen een bijzonder in de belangstelling stel onderwerpen behandelen, welke voor alle geïnteresseerden van grote interesse zullen blijken; het onderwerp houden we echter nog geheim .....

NIEUWE PRIJSSTELLING.

Met ingang van 1 januari 1971 zijn de door ons afgegeven verkoopsprijzen excl. 14% B.T.W. gesteld; de structuur van onze Handelmaatschappij heeft deze verandering noodzakelijk gemaakt. Hierdoor waren wij tevens genoodzaakt een nieuwe prijslijst te maken, welke aan al onze relaties inmiddels is toegezonden. Deze prijslijst heeft niet de pretentie volledig te zijn, terwijl de gepubliceerde prijzen aan veranderingen onderhevig kunnen zijn. Heeft U nog geen prijslijst ontvangen, stuurt U dan een briefkaartje of briefje aan:

N.V. Technische Handelmaatschappij Van Dam Elektronica
Postbus 3149, Rotterdam-3011, Holland

Tot slot wijzen wij U nog op de op pag. 3 opgenomen bestelmethoden; toepassing van de juiste methode brengt voor U en ons gemak met zich mee, waardoor wij onze service kunnen handhaven en, waar nodig, nog verder uitbreiden. Wij zijn tot nog toe bereid elk orderbedrag uit te voeren, mits U Uw medewerking hierbij ook verleent .....

Nieuw voltage regulator **L005**

Op pagina 19 is het datasheet van een geheel nieuw IC opgenomen; dit is Uw aandacht ten zeerste waard! Wij kunnen dit IC ook leveren in 15 volt en 12 volt. Nadere gegevens hierover worden opgenomen in onze uitgave van 1971.

NU OOK IN VOORRAAD: 2 x 25 bits, 2 x 50 bits en 2 x 100 bits MOS shiftregisters.

Bestellen op een moderne manier.

Mede dank zij onze voorraadpositie en levertijd maken steeds meer cliënten regelmatig gebruik van onze service. Wij hebben hierbij altijd getracht, onze service optimaal te laten functioneren en onze cliënten zo deskundig mogelijk te adviseren omtrent het toepassen en verwerken van de door ons aangeboden kwaliteitsartikelen. Dit is een bijzonder tijdrovende bezigheid, doch ook in de toekomst willen wij aan iedereen deze service verlenen en, waar nodig, nog verder uitbreiden. Daarvoor is echter Uw medewerking noodzakelijk ....!!!

Door het steeds intensiever gebruik van gegarandeerde betaalkaarten van de Post-, Cheque- en Girodienst en betaalcheques van de hier ter lande gevestigde bankinstellingen kunt U ons veel tijd besparen door Uw bestellingen op één van de volgende manieren te laten plaatsvinden. U bespaart hiermee al onze afdelingen tijd, hetgeen ter Uwer gunste tot uitdrukking komt in een optimale service, deskundig advies, snelle levertijd en (want: tijd is geld) een concurrerende prijs.

Manier 1. Bestelling door bijvoeging van een gegarandeerde betaalkaart van de PCGD.

Door de Nederlandse Post-, Cheque- en Girodienst worden zonder kosten betaalkaarten tot *f* 100,- per kaart verstrekt aan rekeninghouders, welke nimmer hun saldo overschreden hebben. Over deze kaarten kunt U inlichtingen verkrijgen bij elk PTT kantoor of het girokantoor te Den Haag of Arnhem. Deze kaarten worden tegenwoordig als betaalmiddel aanvaard en zijn reeds in het bezit van zo'n 1.500.000 rekeninghouders. Deze kaarten kunt U, voorzien van ons gironummer (295550), naam (N.V. Technische Handelmaatschappij Van Dam Elektronica), plaats (Rotterdam-3011) en Uw handtekening bij Uw bestelling voegen. Vult U hierbij echter op een kaart géén bedrag in: zou U door prijsfluctuaties of verzendkosten te weinig betaald hebben, dan kunnen wij Uw bestelling niet volledig in behandeling nemen en geeft dit voor U bijzonder veel ongemak! Bij Uw bestelling wordt door ons een volledig gespecificeerde nota gevoegd, terwijl op deze wijze U tevens de tegenwoordig bijzonder opgelopen rembourskosten (*f* 3,14) beperkt tot slechts *f* 0,50-*f* 0,80 voor pakjes tot 250 gram. Daarnaast heeft U Uw bestelling in huis op de werkdag, volgend op de dag, dat wij Uw bestelling ontvangen (dus 1 à 2 dagen nadat U Uw bestelling heeft gepost: adresseer hiertoe uitsluitend aan onze Postbus nr. 3149) en behoeft er niemand thuis te blijven om de postbode te betalen ....! U ontvangt op deze wijze Uw bestelling franco huis, terwijl U na circa 1 week de afschrijving door de Post-, Cheque- en Girodienst wordt toegezonden. Wij kunnen U op deze wijze een snelle service verlenen doordat onze orderafdeling en boekhouding geen rembourskaarten behoeven te verzorgen.

Manier 2. Bestelling door bijvoeging van een gegarandeerde bankcheque.

Ook door de Nederlandse bankinstellingen worden cheques verstrekt aan houders van een rekening-courant. Deze cheques zijn eveneens gegarandeerd tot *f* 100,-. Over deze betaalcheques kunt U bij Uw bankrelatie nadere informaties verkrijgen. Op deze cheques, welke U ook bij Uw bestelling kunt voegen, dienen onze naam (N.V. Technische Handelmaatschappij Van Dam Elektronica) en Uw handtekening te worden geplaatst. Ook hierbij dient U op één kaart geen bedrag in te vullen, zodat het juiste bedrag door ons kan worden ingevuld. De verdere afwikkeling van Uw opdracht vindt plaats als onder "manier 1." is aangegeven, terwijl U na enige tijd een afrekening van Uw bankrelatie ontvangt.

Manier 3. De kostbare manier voor levering onder rembours.

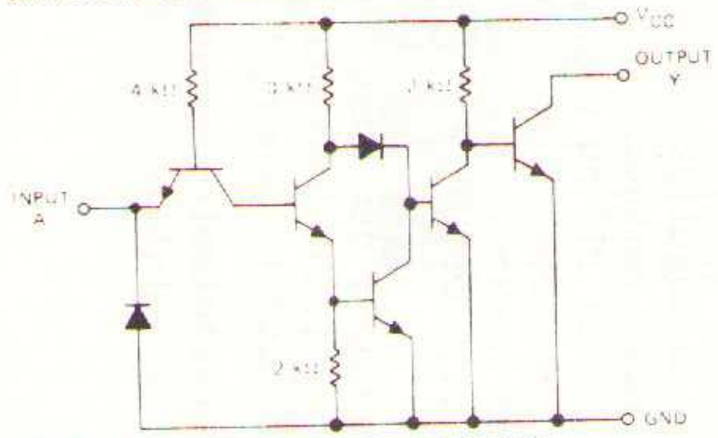
Kunt U geen gebruik maken van de onder manier 1 en 2 opgegeven mogelijkheden, dan kunnen wij Uw bestelling, mits het totaalbedrag boven *f* 15,- is, onder rembours uitvoeren; hierbij bent U aan verzendkosten *f* 3,14 of meer kwijt (dat vraagt de PTT nu eenmaal...), terwijl U voor bedragen onder *f* 25,- bovendien *f* 1,50 extra voor verpakkingskosten in rekening wordt gebracht. Vraagt U daarom ook een girorekening of bankrelening aan: het is zo gemakkelijk, het bespaart U geld en U krijgt nog rente ook .....

Wilt U Uw bestelling per expresse of aangetekend laten verzenden, dan kunt U dit bij Uw bestelling aangeven; de extra portokosten bedragen hiervoor *f* 1,25. Door ons gironummer en onze naam op Uw kaart aan te geven hebben deze voor buitenstaanders generlei waarde.

Wij zijn ervan overtuigd, dat de onder 1. en 2. aangegeven bestelmethoden voor U en ons een groter gemak met zich mee zullen brengen en rekenen op Uw welwillende medewerking hierbij; uiteindelijk is dit ook in Uw voordeel .....

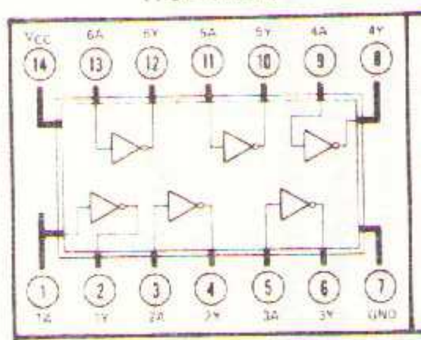
FOR INTERFACING WITH HIGH-LEVEL CIRCUITS
OR FOR DRIVING HIGH-CURRENT LOADS

schematic (each inverter)

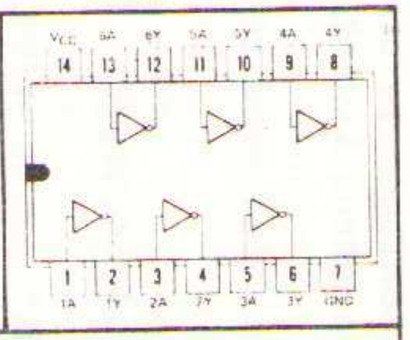


NOTE: Component values shown are nominal.

S
FLAT PACKAGE
(TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A}$

- Converts TTL voltage levels to MOS levels
- High sink-current capability
- Input clamping diodes simplify system design
- Typical propagation delay time: 15 ns
- Open-collector driver for indicator lamps and relays
- Inputs fully compatible with most TTL and DTL circuits
- Typical power dissipation: 105 mW

description

These monolithic TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as inverter buffers for driving TTL inputs. For increased fan-out, several inverters in a single package may be paralleled. The SN5406 and SN7406 have minimum breakdown voltages of 30 volts and the SN5416 and SN7416 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5406 and SN5416, and 40 milliamperes for the SN7406 and SN7416.

These circuits are completely compatible with most TTL or DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 150 milliwatts and average propagation delay time is 15 nanoseconds. The SN5406 and SN5416 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7406 and SN7416 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Output voltage (see Notes 1 and 2): SN5406, SN7406 Circuits . . . . . 30 V
SN5416, SN7416 Circuits . . . . . 15 V
Operating free-air temperature range: SN5406, SN5416 Circuits . . . . . −55°C to 125°C
SN7406, SN7416 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5406, SN5416			SN7406, SN7416			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	SN5406, SN7406			30			30	V
	SN5416, SN7416			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1		2			V
V_{IL}	Low-level input voltage	2				0.8	V
I_{OH}	High-level output current	2	V_{CC} = MIN, V_I = 0.8 V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_I = 2 V, I_{OL} = MAX			0.7	V
			V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	5	V_{CC} = MAX, V_I = 0		30	42	mA
I_{CCL}	Supply current, low-level output	5	V_{CC} = MAX, V_I = 5 V		27	38	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 15 pF, R_L = 110 Ω		17	26	ns
t_{PHL}	Propagation delay time, high-to-low-level output	6	C_L = 15 pF, R_L = 110 Ω		13	20	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

d-c test circuits§

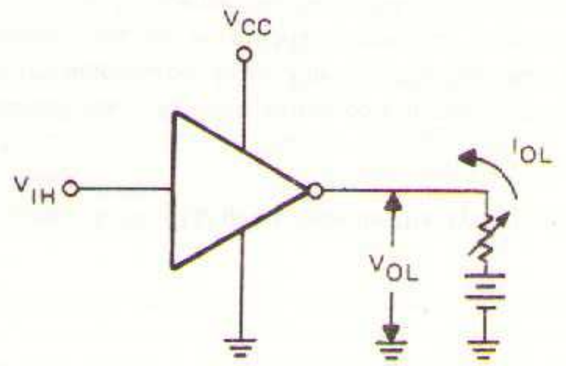


FIGURE 1–V_{IH}, V_{OL}

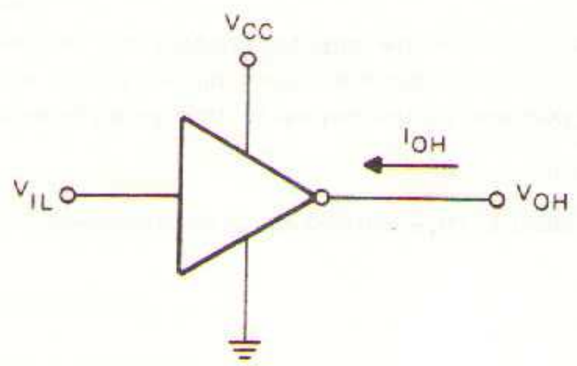


FIGURE 2–V_{IL}, I_{OH}

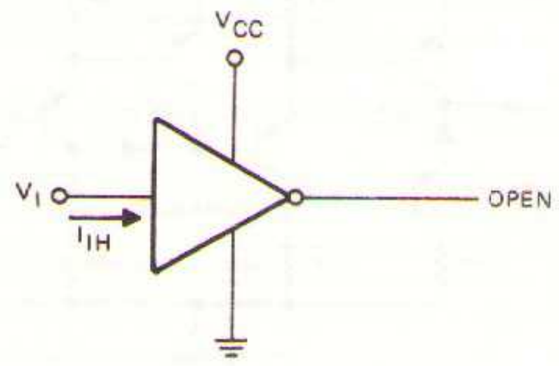


FIGURE 3–I_{IH}

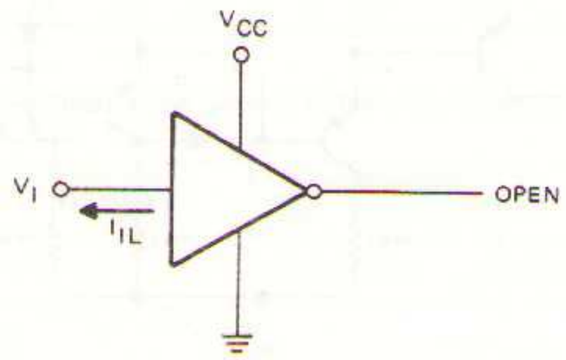
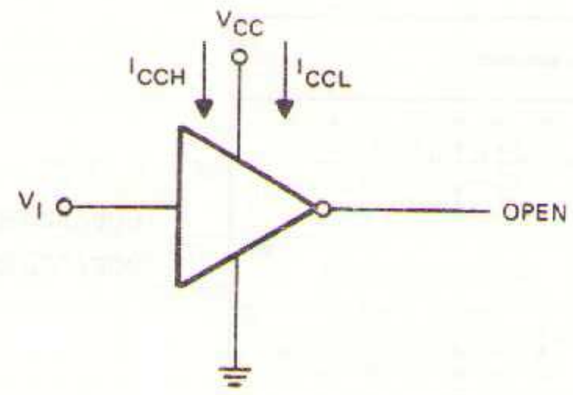


FIGURE 4–I_{IL}

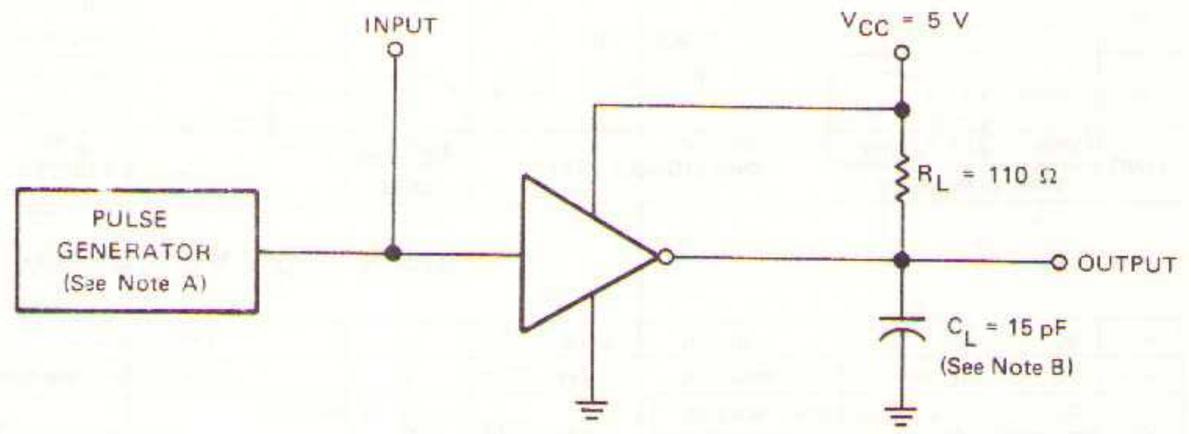


All inverters are tested simultaneously.

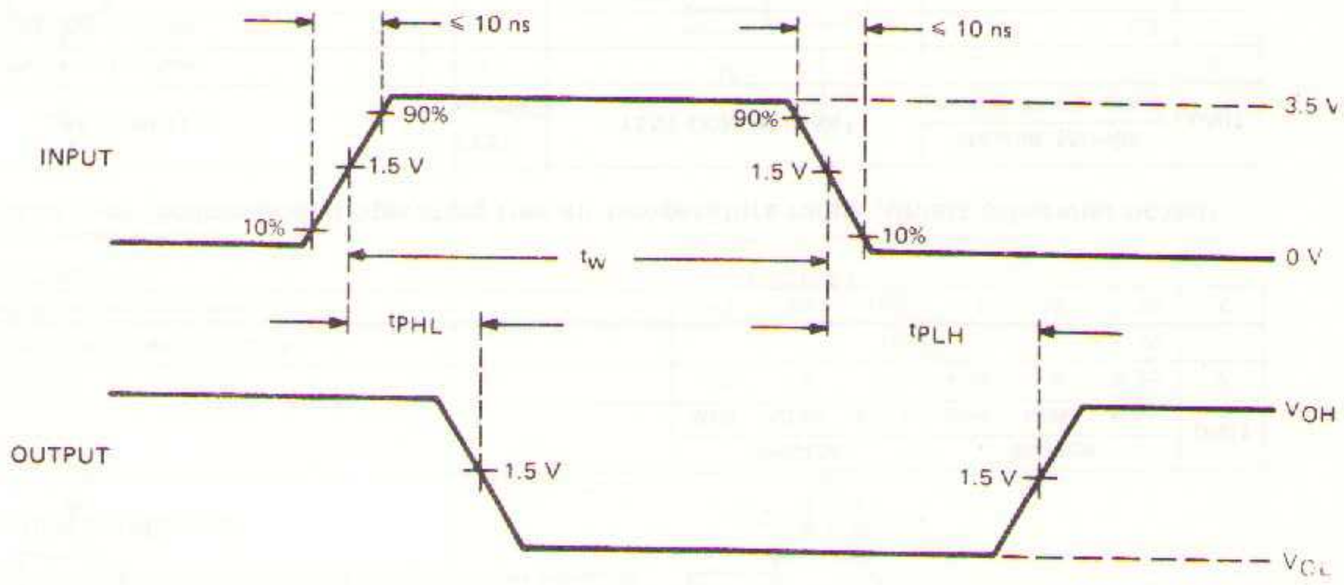
FIGURE 5–I_{CCH}, I_{CCL}

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

switching characteristics



TEST CIRCUIT

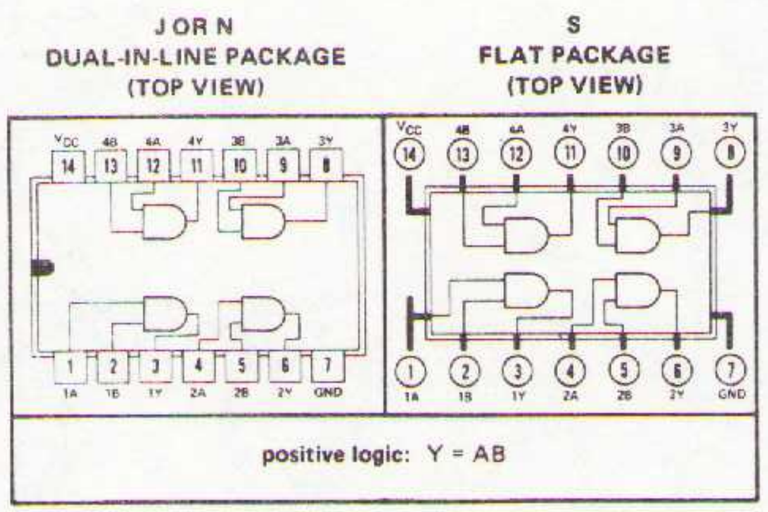


VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

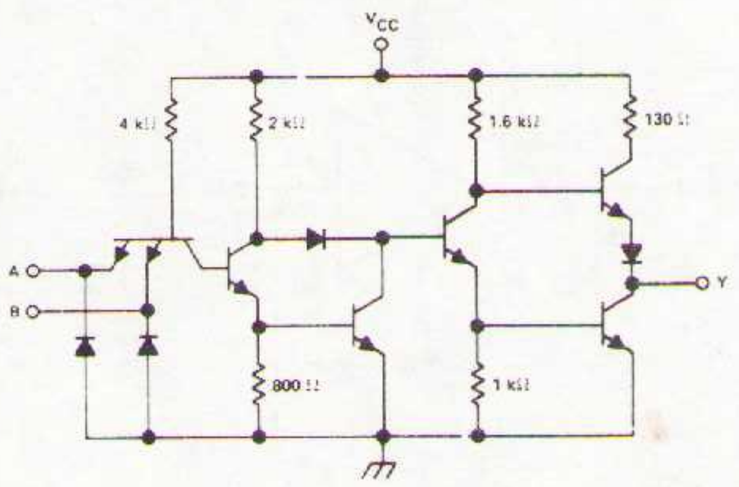
FIGURE 6–PROPAGATION DELAY TIMES

Choice of Totem-Pole Outputs (SN5408/SN7408)
or Open-Collector Outputs (SN5409/SN7409)

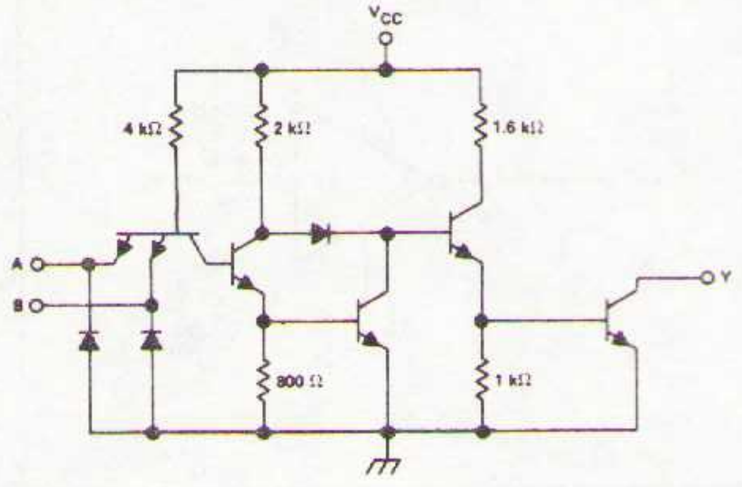


schematics (each gate)

SN5408, SN7408



SN5409, SN7409



Component values shown are nominal.

description

These Series 54/74 TTL gates provide the system designer with direct implementation of the positive AND or negative OR functions.

The SN5408/SN7408, with totem-pole outputs, drives 10 normalized Series 54/74 loads at the low output level and 20 loads at the high output level. The SN5409/SN7409, with open-collector output, provides additional logic flexibility, as the outputs may be wire-AND connected to extend the AND function. The SN5409/SN7409 will sink sufficient current to drive 10 normalized Series 54/74 loads at the low output level.

The SN5408 and SN5409 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7408 and SN7409 are characterized for operation from 0°C to 70°C.

SN5408, SN7408

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range, T_A: SN5408 Circuits	−55°C to 125°C
SN7408 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	SN5408			SN7408			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN5408, SN7408 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	3					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	3	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX,	V_I = 2.4 V			40	μA
			V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	5	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	6	V_{CC} = MAX	SN5408	−20		−55	mA
				SN7408	−18		−55	
I_{CCH}	Supply current, high-level output	7	V_{CC} = MAX,	V_I = 5 V		10	15	mA
I_{CCL}	Supply current, low-level output	7	V_{CC} = MAX,	V_I = 0		18	26	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5408, SN7408 MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	8	C_L = 15 pF, R_L = 400 Ω		17.5	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	19	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be sh[illegible]at a time.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Interemitter voltage (see Note 2)		5.5 V
Output voltage (see Notes 1 and 3)		5.5 V
Operating free-air temperature range:	SN5409 Circuits	−55°C to 125°C
	SN7409 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5409			SN7409			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	SN5409, SN7409 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	2		2			V
V_{IL}	Low-level input voltage	3				0.8	V
I_{OH}	High-level output current	2	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	3	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	5	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	7	V_{CC} = MAX, V_I = 5 V	10	15		mA
I_{CCL}	Supply current, low-level output	7	V_{CC} = MAX, V_I = 0	18	26		mA

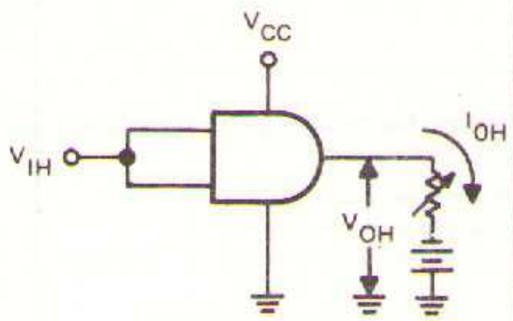
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5409, SN7409 MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	8	C_L = 15 pF, R_L = 400 Ω		21	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output				16	24	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



Both inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OH}

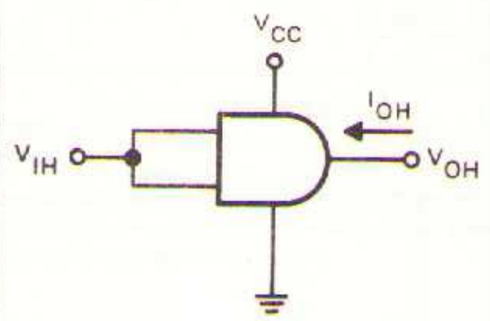
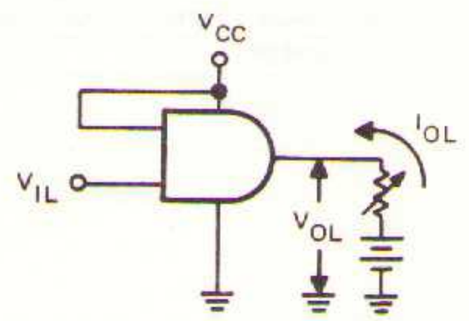
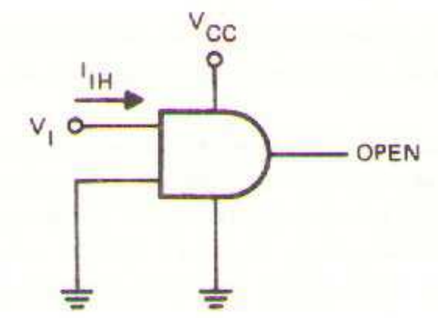


FIGURE 2–V_{IH}, I_{OH}



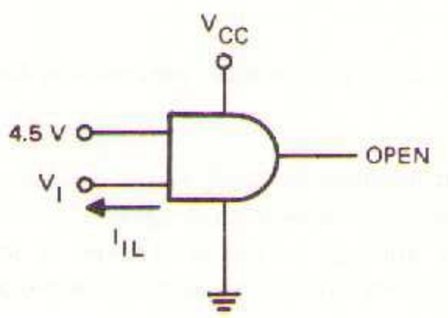
Each input is tested separately.

FIGURE 3–V_{IL}, V_{OL}



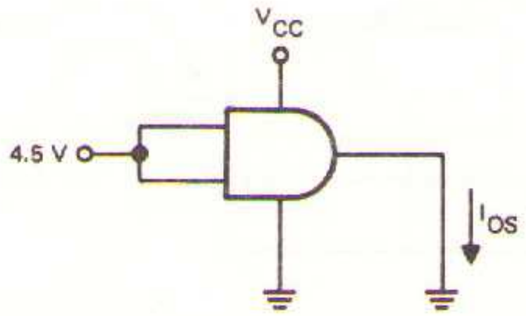
Each input is tested separately.

FIGURE 4–I_{IH}



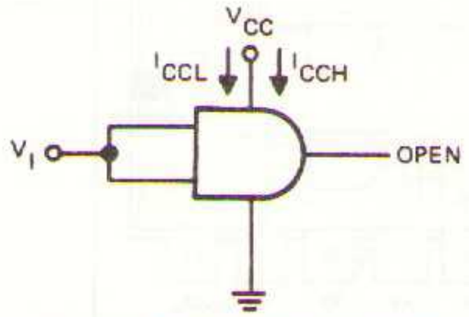
Each input is tested separately.

FIGURE 5–I_{IL}



Each gate is tested separately.

FIGURE 6–I_{OS}



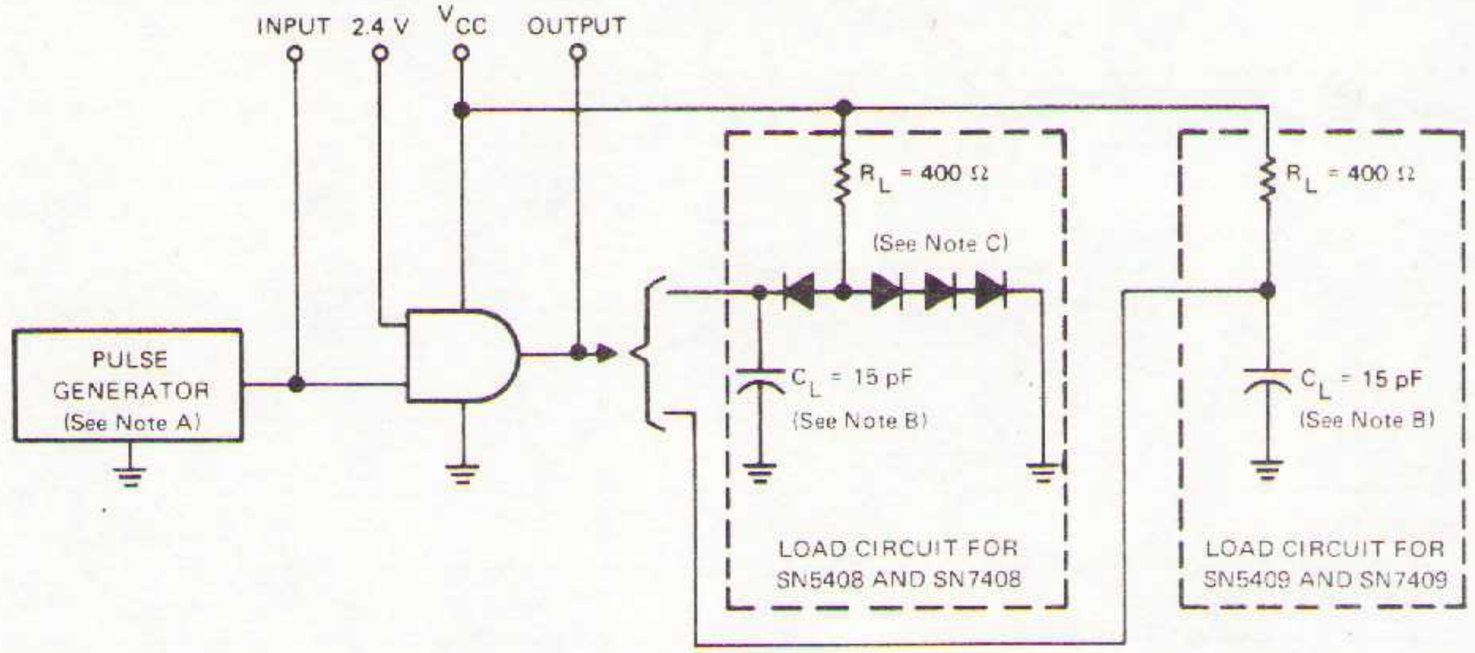
A. High-level and low-level conditions are tested.
B. All gates are tested simultaneously.

FIGURE 7–I_{CCH}, I_{CCL}

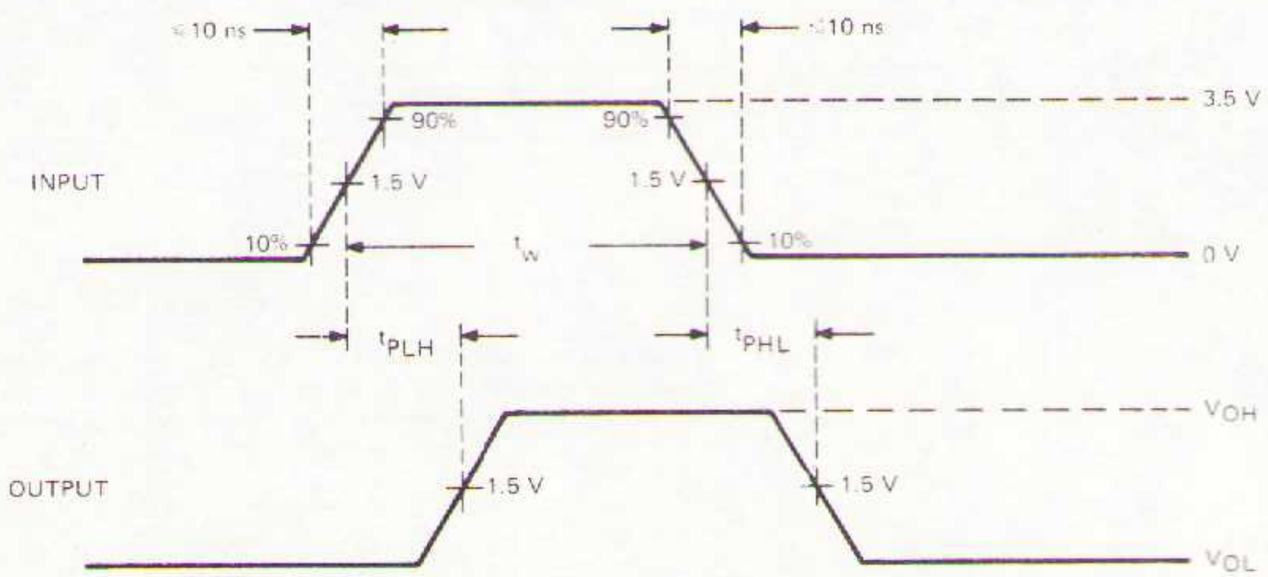
¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



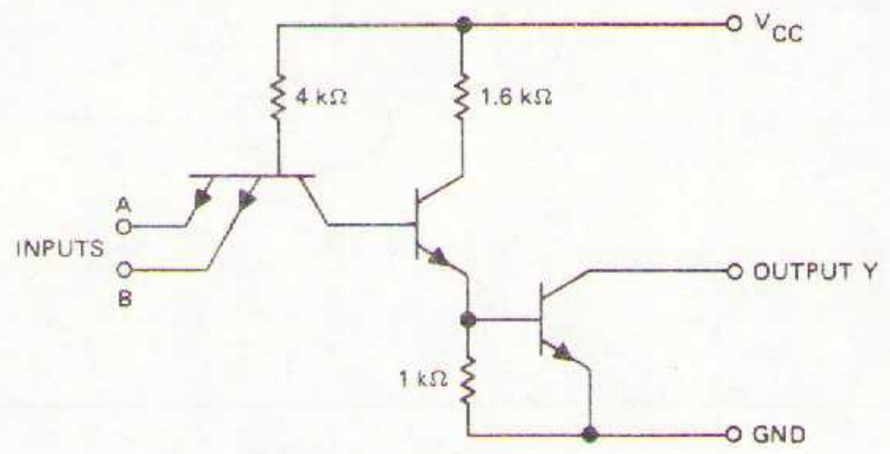
VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 8–PROPAGATION DELAY TIMES

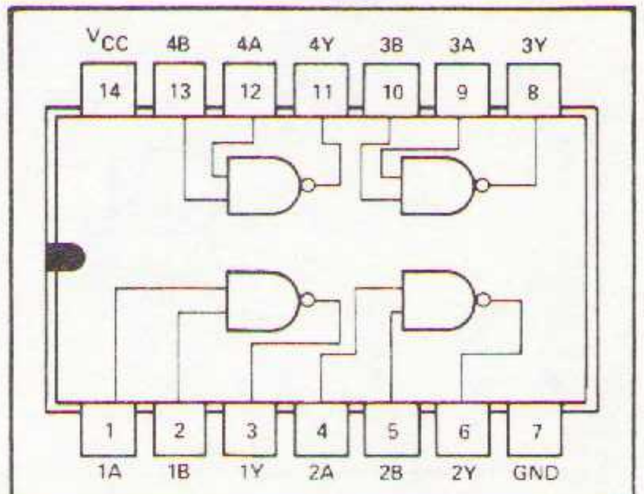
FOR DRIVING LOW-THRESHOLD-VOLTAGE MOS INPUTS

schematic (each gate)



Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

These open-collector NAND gates feature high output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the V_{CC} terminal is connected to the standard 5-volt source. The output transistor will sink 16 milliamperes while maintaining a low-level output voltage of 0.4 volt maximum thus providing a high-fan-out driver with the nominal power dissipation of standard Series 54/74 gates.

The SN5426 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7426 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Notes 1 and 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3) . . . . . 15 V
Operating free-air temperature range: SN5426 Circuits . . . . . −55°C to 125°C
SN7426 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5426			SN7426			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}			15			15	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	1		2			V
V_{IL}	Low-level input voltage	2				0.8	V
V_{OH}	High-level output voltage	2	V_{CC} MIN, V_{IL} 0.8 V, I_{OH} 1 mA	15			V
I_{OH}	High-level output current	2	V_{CC} MIN, V_{IL} 0.8 V, V_{OH} 12 V			50	μA
V_{OL}	Low-level output voltage	1	V_{CC} MIN, V_{IH} 2 V, I_{OL} 16 mA			0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} MAX, V_I 2.4 V			40	μA
			V_{CC} MAX, V_I 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} MAX, V_I 0.4 V			1.6	mA
I_{CCH}	Supply current, high level output	5	V_{CC} MAX, V_I 0		4	8	mA
I_{CCL}	Supply current, low level output	5	V_{CC} MAX, V_I 5 V		12	22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

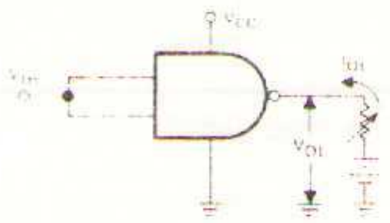
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 15 pF, R_L = 1 kΩ		16	24	ns
t_{PHL}	Propagation delay time, high-to-low-level output	6	C_L = 15 pF, R_L = 1 kΩ		11	17	ns

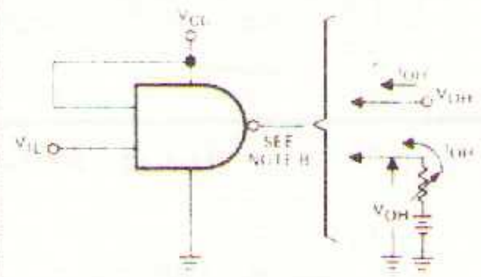
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



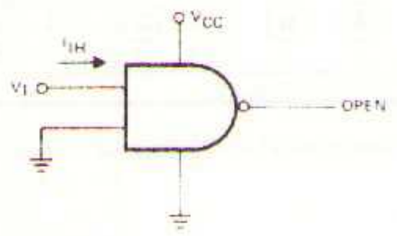
Both inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OL}



A. Each input is tested separately.
B. I_{OH} is tested at V_{OH} = 12 V and V_{OH} is tested at I_{OH} = 1 mA.

FIGURE 2–V_{IL}, V_{OH}, I_{OH}



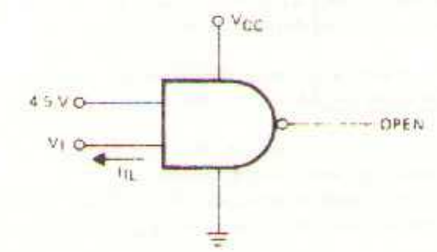
Each input is tested separately.

FIGURE 3–I_{IH}

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

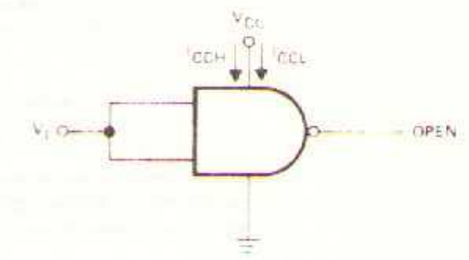
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



Each input is tested separately.

FIGURE 4–I_{IL}

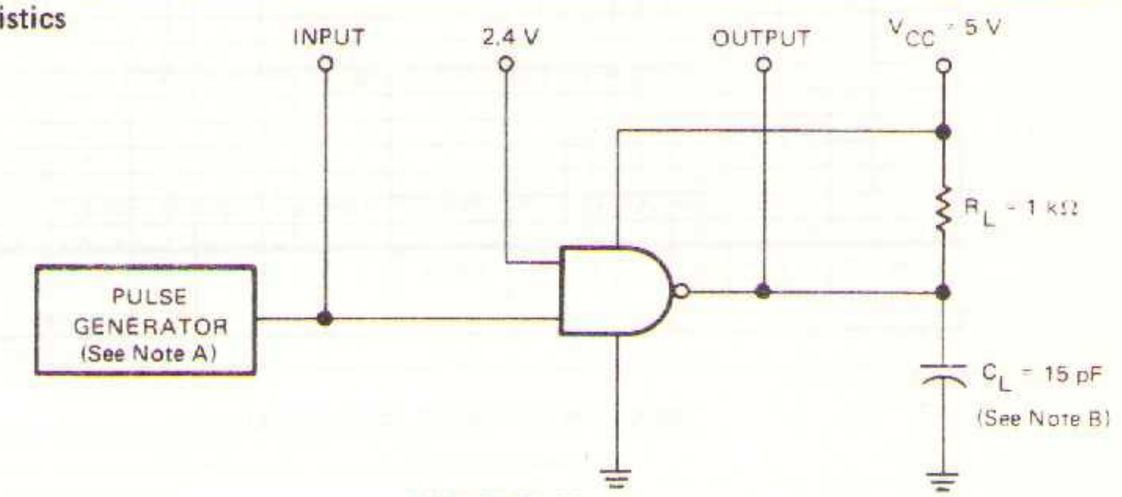


High-level and low-level output conditions are tested.

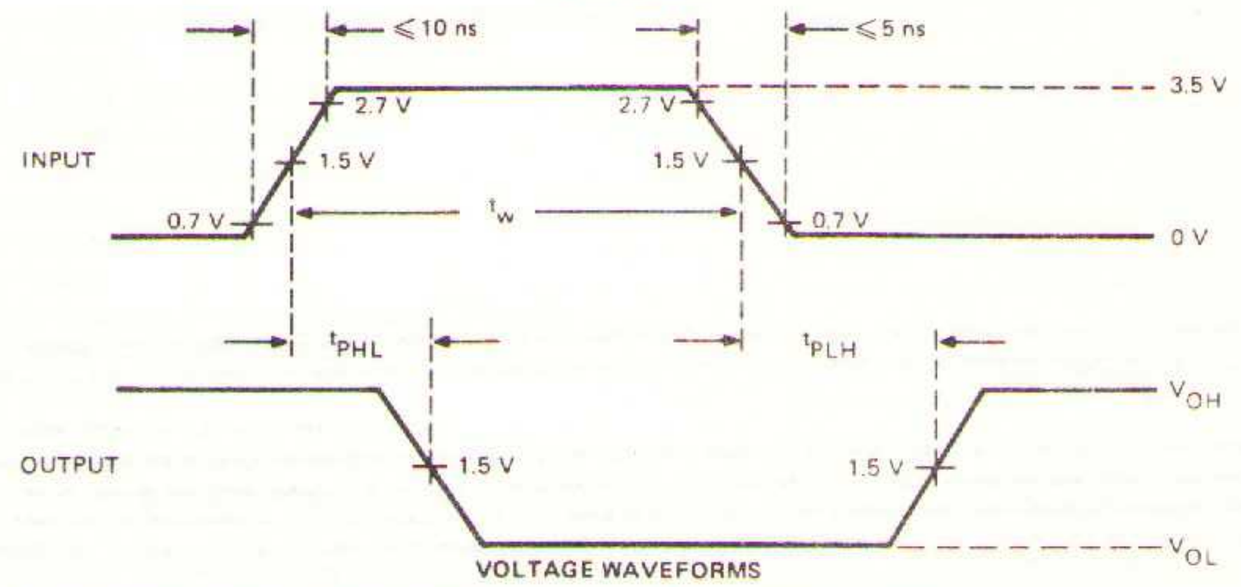
FIGURE 5–I_{CCH}, I_{CCL}

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 6–PROPAGATION DELAY TIMES

SN5446, SN5447, SN7446 SN7447
featuring

- DIRECT DRIVE FOR INDICATORS
- OPEN COLLECTOR OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- CERAMIC OR PLASTIC DUAL IN LINE PACKAGES

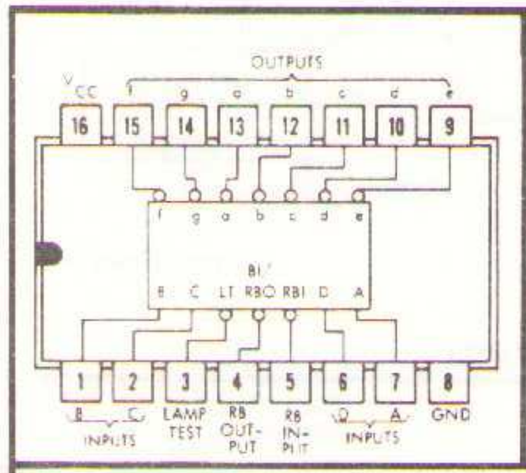
SN5448, SN7448
featuring

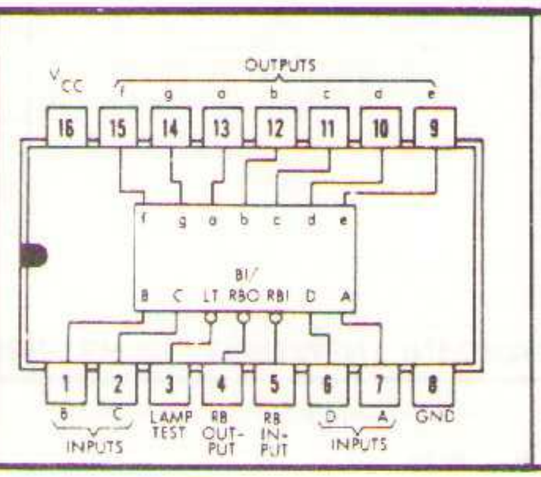
- PASSIVE PULL-UP OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- CERAMIC OR PLASTIC DUAL IN-LINE PACKAGES

SN5449, SN7449
featuring

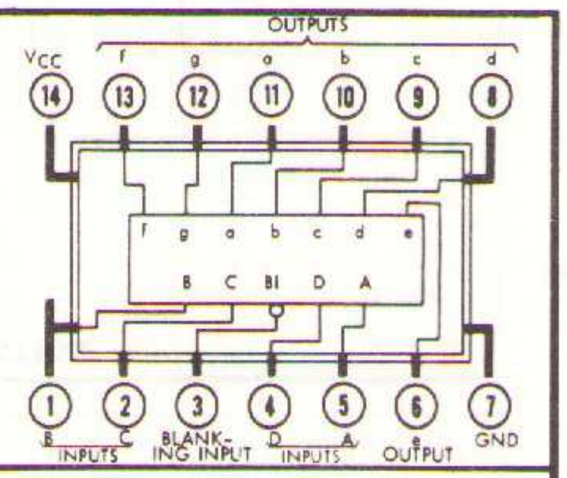
- OPEN-COLLECTOR OUTPUTS
- BLANKING INPUT
- WELDED FLAT PACKAGE

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)





S FLAT PACKAGE (TOP VIEW)



positive logic: see truth tables

ALL CIRCUIT TYPES FEATURE:

- TTL-DTL COMPATIBILITY
- FULL DECODING OF ALL 16 INPUT COMBINATIONS
- LAMP INTENSITY MODULATION CAPABILITY

description

These monolithic, TTL, BCD-to-seven-segment decoder/drivers consist of NAND gates, input buffers, and seven AND-OR-INVERT gates. Three configurations offer active-low, high-sink-current outputs (SN5446 and SN5447) for driving indicators directly; active-high, passive-pull-up outputs, (SN5448) and active-high, open-collector outputs (SN5449) for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR gates, and the remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output, and ripple-blanking input for the SN5446, SN5447 and SN5448. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the SN5449. See functional block diagrams.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a seven-segment display indicator (SN5446 and SN5447) or other components (SN5448, SN5449). The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN5446 and SN5447 are designed to withstand the relatively high voltages required for seven segment indicators. The SN5446 outputs will withstand 30 volts, and the SN5447 will withstand 15 volts, with a maximum reverse current of 250 microamperes. Indicator segments requiring up to 20 milli-amperes of current may be driven directly from the SN5446 or SN5447 high-performance output transistors. Segment identification with resultant displays are shown in Figure A. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The SN5446, SN5447, and SN5448 circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is a logical 1. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs. All inputs except the BI/RBO nodes are one normalized series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs. Power dissipation is typically 265 milliwatts (SN5446, SN5447, and SN5448) or 165 milliwatts (SN5449).

The SN5446, SN5447, SN5448 and SN5449 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7446, SN7447, SN7448, and SN7449 (electrically identical to the corresponding Series 54 types) are for operation over the temperature range of 0°C to 70°C.

TRUTH TABLE SN5446, SN5447, SN7446, SN7447

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1	
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0	4

NOTES: 1. BI/RBO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.

2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.

3. When ripple-blanking input (RBI) is at a logical 0 and A=B=C=D=logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).

4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

TRUTH TABLE SN5448, SN7448

DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

NOTES: 1. BI/RBO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 output. X=input may be high or low.

2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.

3. When ripple-blanking input (RBI) is at a logical 0, and A=B=C=D=logical 0, all segment outputs go to a logical 0 and the ripple-blanking output goes to a logical 0 (response condition).

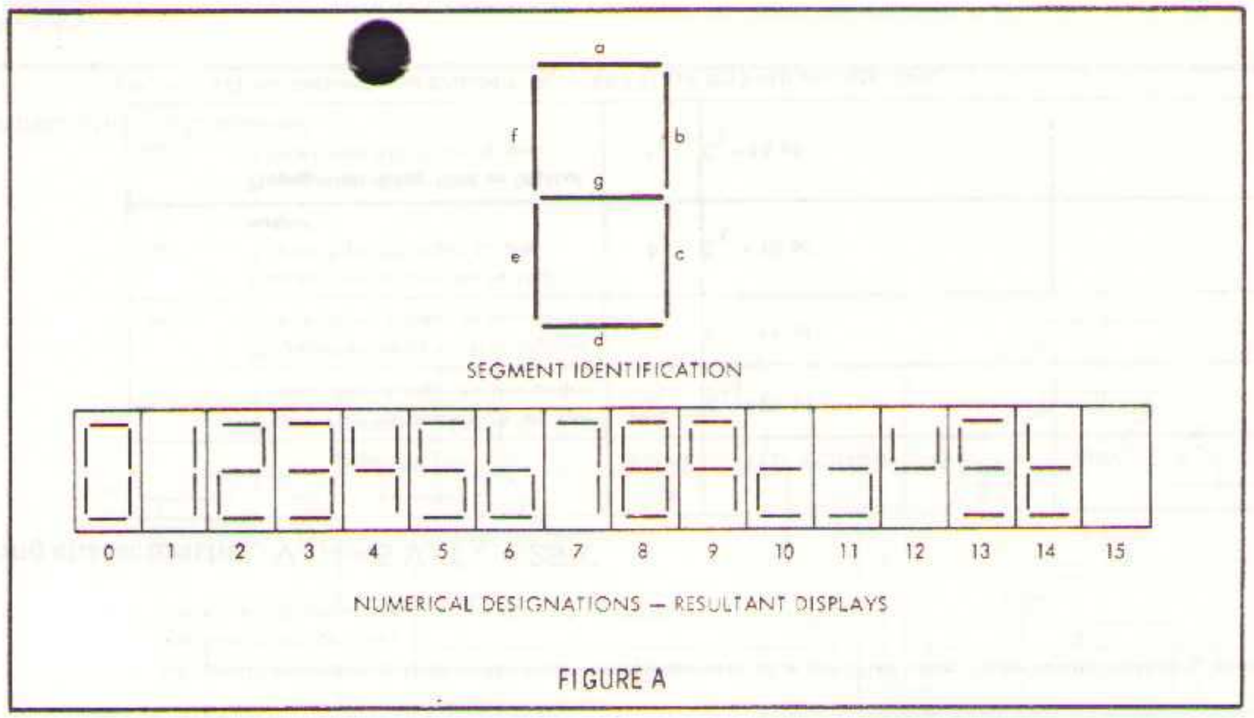
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 1.

TRUTH TABLE SN5449, SN7449

DECIMAL OR FUNCTION	D	C	B	A	BI	a	b	c	d	e	f	g	NOTE
0	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	1	0	1	1	0	0	1	1	
5	0	1	0	1	1	1	0	1	1	0	1	1	
6	0	1	1	0	1	0	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	0	0	0	0	0	0	0	0	2

NOTES: 1. The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired.

2. When a logical 0 is applied to the blanking input all segment outputs go to a logical 0 regardless of the state of any other input condition. X = input may be high or low.



SEGMENT IDENTIFICATION

NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

FIGURE A

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Current Into any Output of SN5446, SN7446, SN5447, SN7447, SN5449, SN7449 (See Note 3) . . . . . 1 mA
Operating Case Temperature Range: SN5449 Circuits . . . . . −55°C to 125°C
Operating Free-Air Temperature Range:
SN5446, SN5447, SN5448 Circuits . . . . . −55°C to 125°C
SN7446, SN7447, SN7448, SN7449 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):				
SN5446, SN5447, SN5448, SN5449 Circuits	4.5	5	5.5	V
SN7446, SN7447, SN7448, SN7449 Circuits	4.75	5	5.25	V
Continuous Voltage at Outputs a through g:				
SN5446, SN7446 Circuits			30	V
SN5447, SN7447 Circuits			15	V
SN5449, SN7449 Circuits			5.5	V
Normalized Fan-Out From Outputs a through g to Series 54/74 Loads:				
SN5446, SN7446, SN5447, SN7447 Circuits			12	
SN5448, SN7448 Circuits			4	
SN5449, SN7449 Circuits			6	
Normalized Fan-Out From BI/RBO Node to Series 54/74 Loads:				
SN5446, SN7446, SN5447, SN7447, SN5448, SN7448 Circuits			5	
Output Sink Current, I_{sink}:				
SN5446, SN7446, SN5447, SN7447 Outputs a through g			20	mA
SN5448, SN7448 Outputs a through g			6.4	mA
SN5449, SN7449 Outputs a through g			10	mA
SN5446, SN7446, SN5447, SN7447, SN5448, SN7448 BI/RBO Node			8	mA

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1 and 2	V_{CC}=MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1 and 2	V_{CC}=MIN				0.8	V
V_{on}	On-state output voltage at outputs a through g	1	V_{CC}=MIN, I_{sink}=20 mA			0.27	0.4	V
$V_{out(0)}$	Logical 0 output voltage at BI/RBO node	1	V_{CC}=MIN, I_{sink}=8 mA			0.3	0.4	V
V_{off}	Off-state output voltage at outputs a through g (SN5446 and SN7446 only)	2	V_{CC}=MAX, I_{off}=250 µA		30			V
V_{off}	Off-state output voltage at outputs a through g (SN5447 and SN7447 only)	2	V_{CC}=MAX, I_{off}=250 µA		15			V
$V_{out(1)}$	Logical 1 output voltage at BI/RBO node	2	V_{CC}=MIN, I_{load}=-200 µA		2.4	3.7		V
$I_{in(0)}$	Logical 0 level input current at any input except BI/RBO node	3	V_{CC}=MAX, V_{in}=0.4 V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node	3	V_{CC}=MAX, V_{in}=0.4 V				-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except BI/RBO node	4	V_{CC}=MAX, V_{in}=2.4 V				40	µA
			V_{CC}=MAX, V_{in}=5.5 V				1	mA
I_{OS}	Short-circuit output current at BI/RBO node	5	V_{CC}=MAX				-4	mA
I_{CC}	Supply current	4	V_{CC}=MAX	SN5446, SN5447		53	76	mA
				SN7446, SN7447		53	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	6	C_L = 15 pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	6	C_L = 15 pF, R_L = 280 Ω			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	6	C_L = 15 pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	6	C_L = 15 pF, R_L = 280 Ω			100	ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	1 and 2	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	1 and 2	V_{CC} = MIN			0.8	V
$V_{out(0)}$	Logical 0 output voltage at any output (SN5448, SN7448 only)	1	V_{CC} = MIN, I_{sink} = MAX		0.27	0.4	V
V_{on}	On-state output voltage at any output (SN5449, SN7449 only)	1	V_{CC} = MIN, I_{sink} = MAX		0.27	0.4	V
$V_{out(1)}$	Logical 1 level output voltage at outputs a through g (SN5448, SN7448)	2	V_{CC} = MIN, I_{load} = -400 µA	2.4	4.2		V
$V_{out(1)}$	Logical 1 level output at BI/RBO node (SN5448, SN7448 only)	2	V_{CC} = MIN, I_{load} = -200 µA	2.4	3.7		V
I_{load}	Load current available at outputs a through g (SN5448, SN7448 only)	2	V_{CC} = MIN, V_{out} = 0.85 V	-1.3	-2		mA
V_{off}	Off-state output voltage at any output (SN5449, SN7449 only)	2	V_{CC} = MAX, I_{off} = 250 µA	5.5			V
$I_{in(0)}$	Logical 0 level input current at any input (except BI/RBO node of SN5448, SN7448)	3	V_{CC} = MAX, V_{in} = 0.4 V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node (SN5448, SN7448 only)	3	V_{CC} = MAX, V_{in} = 0.4 V			-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input (except BI/RBO node of SN5448, SN7448)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	µA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at any output (except outputs a through g of SN5449, SN7449)	5	V_{CC} = MAX			-4	mA
I_{CC}	Supply current	4	SN5448		53	76	mA
			SN7448		53	90	mA
			SN5449		33	47	mA
			SN7449		33	56	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the applicable device type.

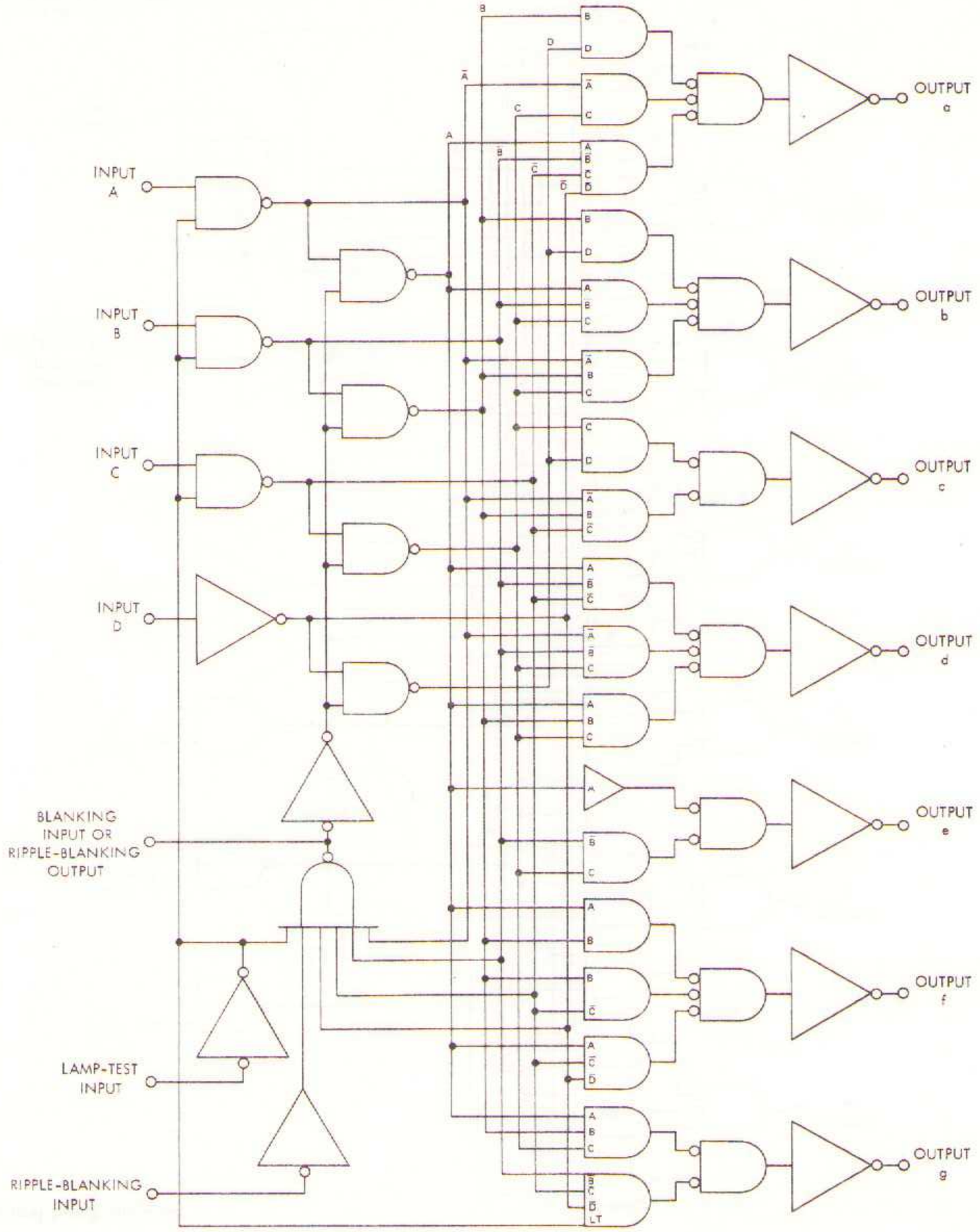
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics, V_{CC} = 5 V, T_A = 25°C

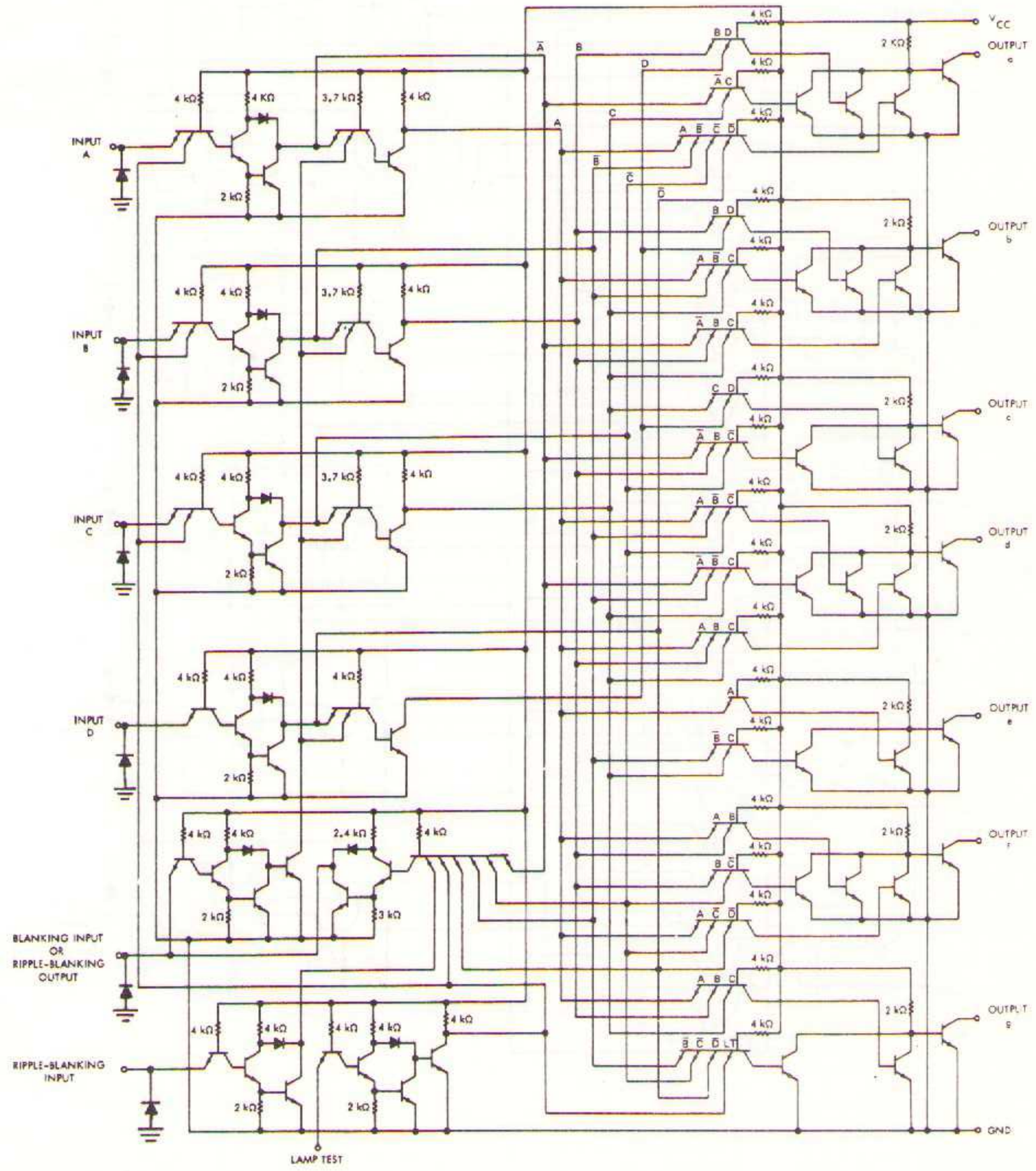
PARAMETER		TEST FIGURE	TEST CONDITIONS §	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	6	C_L = 15 pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	6	C_L = 15 pF			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	6	C_L = 15 pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	6	C_L = 15 pF			100	ns

§ R_L = 1 kΩ for SN5448 and SN5449; R_L = 667 Ω for SN7448 and SN7449.

functional block diagram

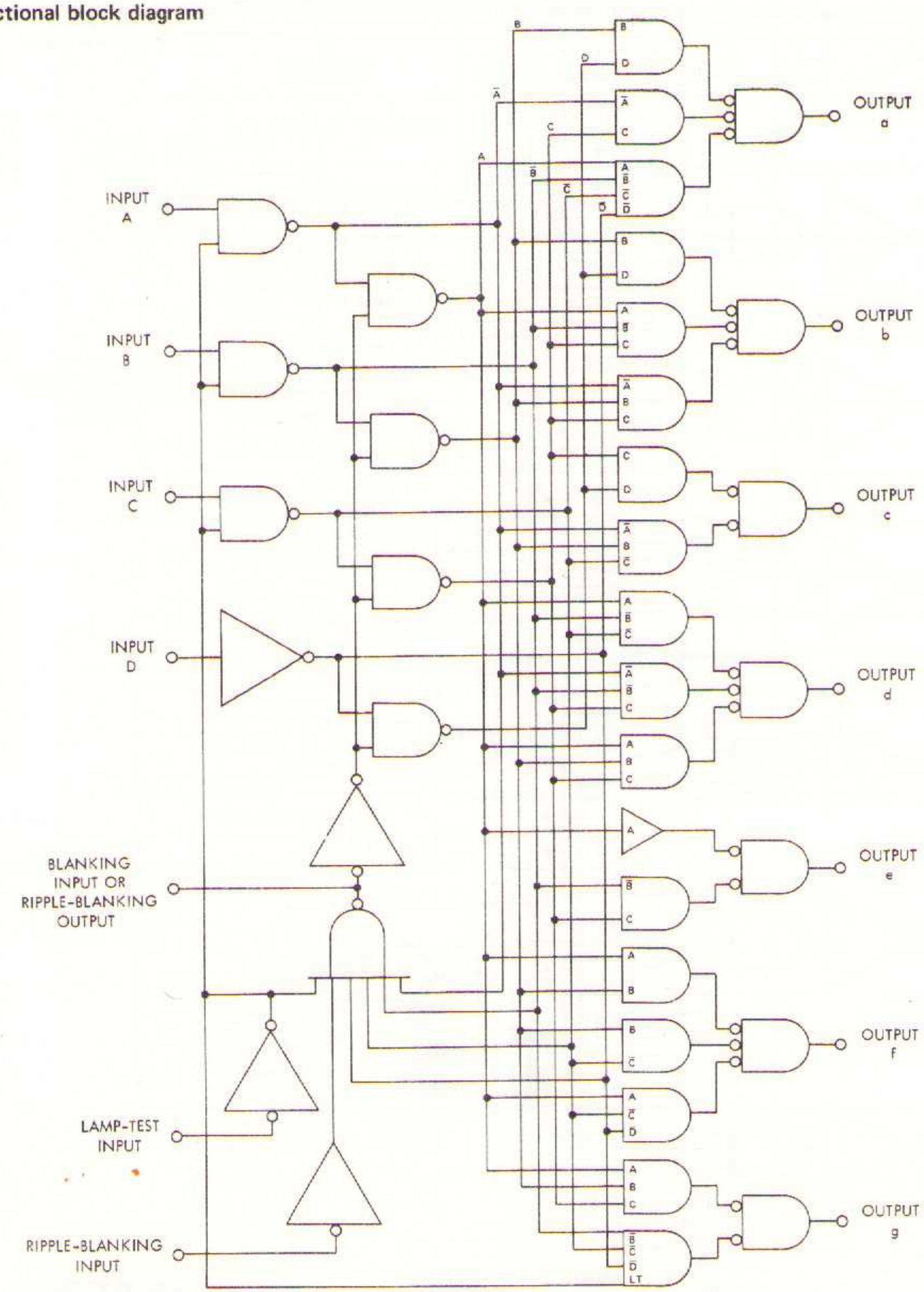


schematic diagram

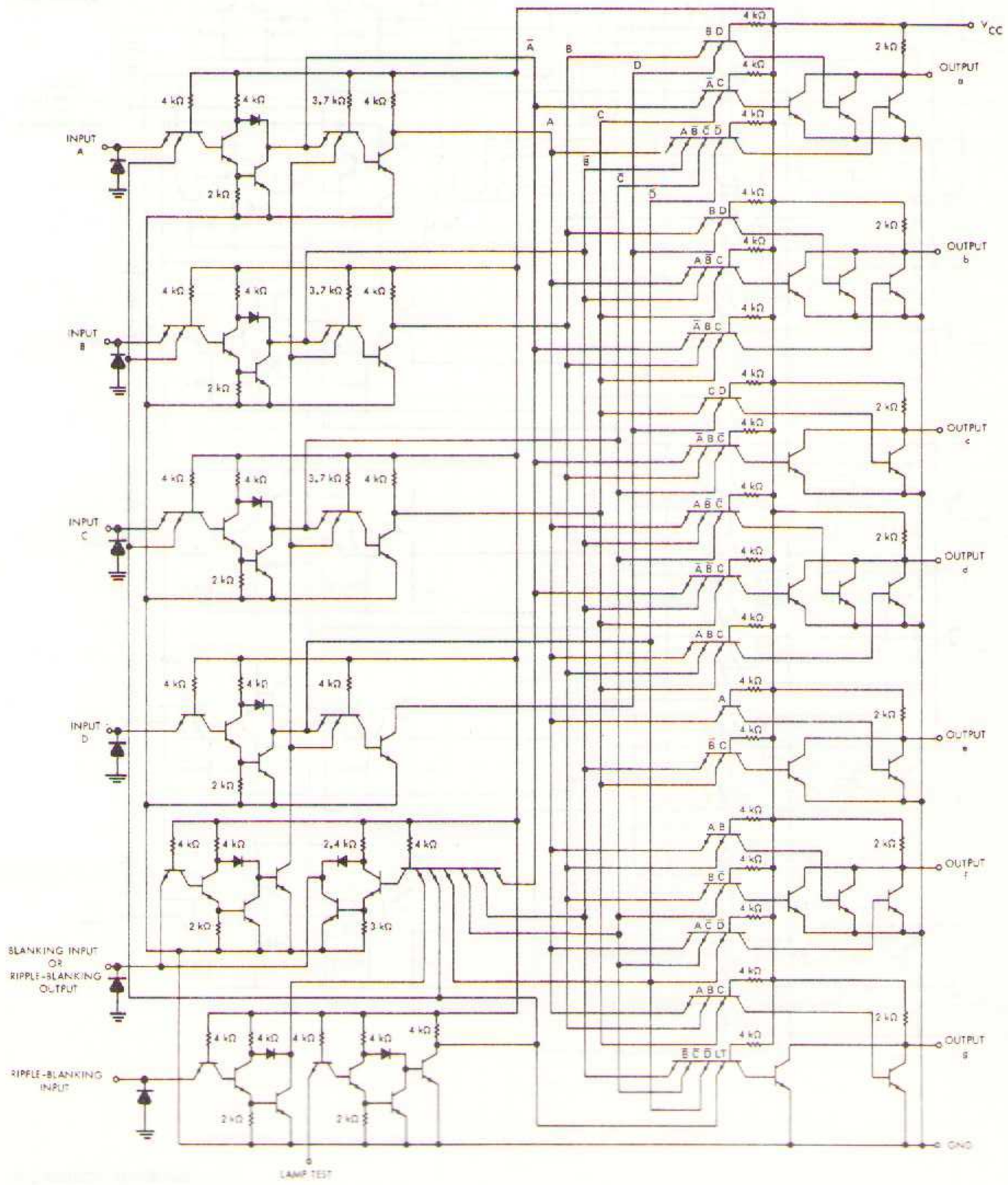


Component values shown are nominal

functional block diagram

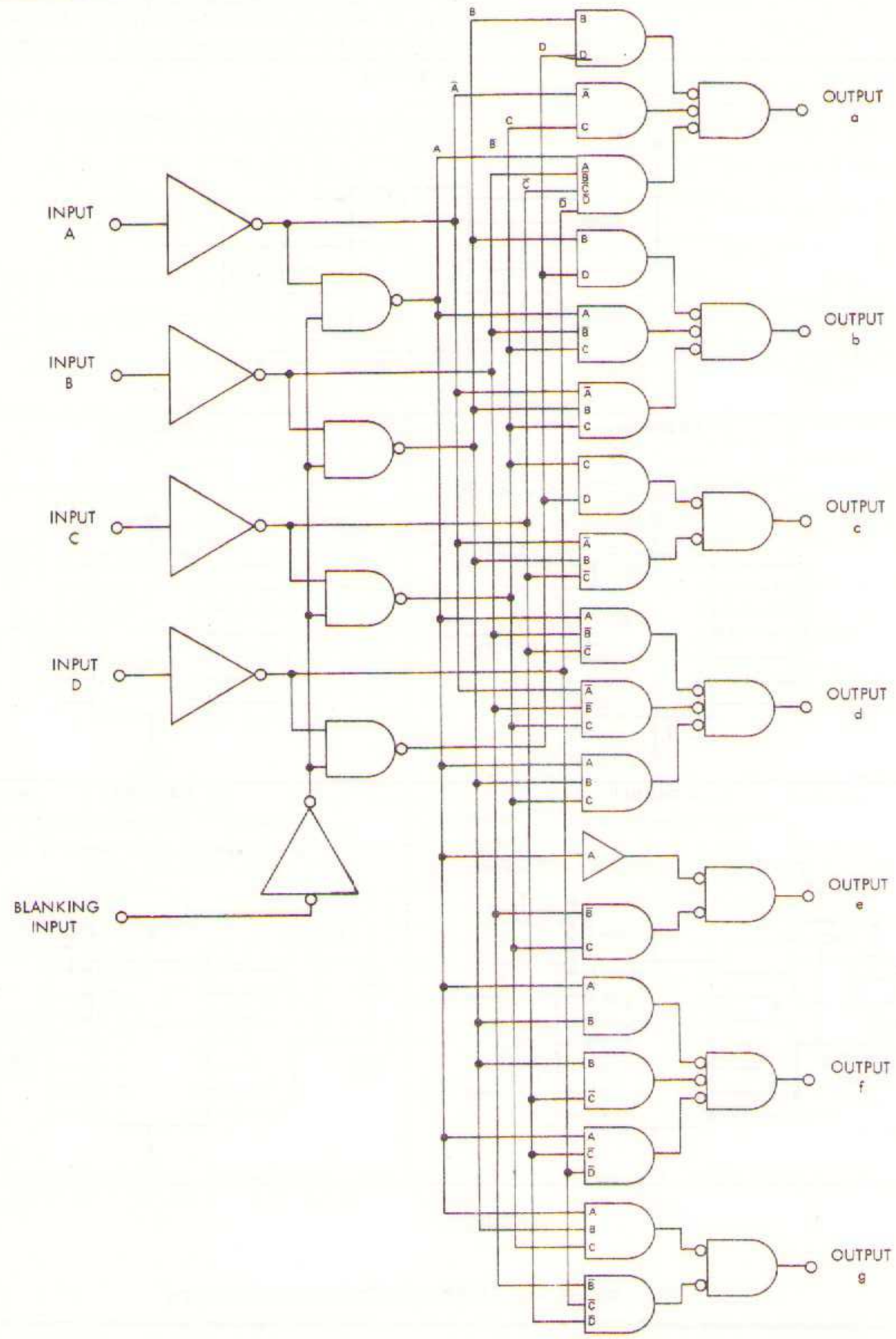


schematic diagram

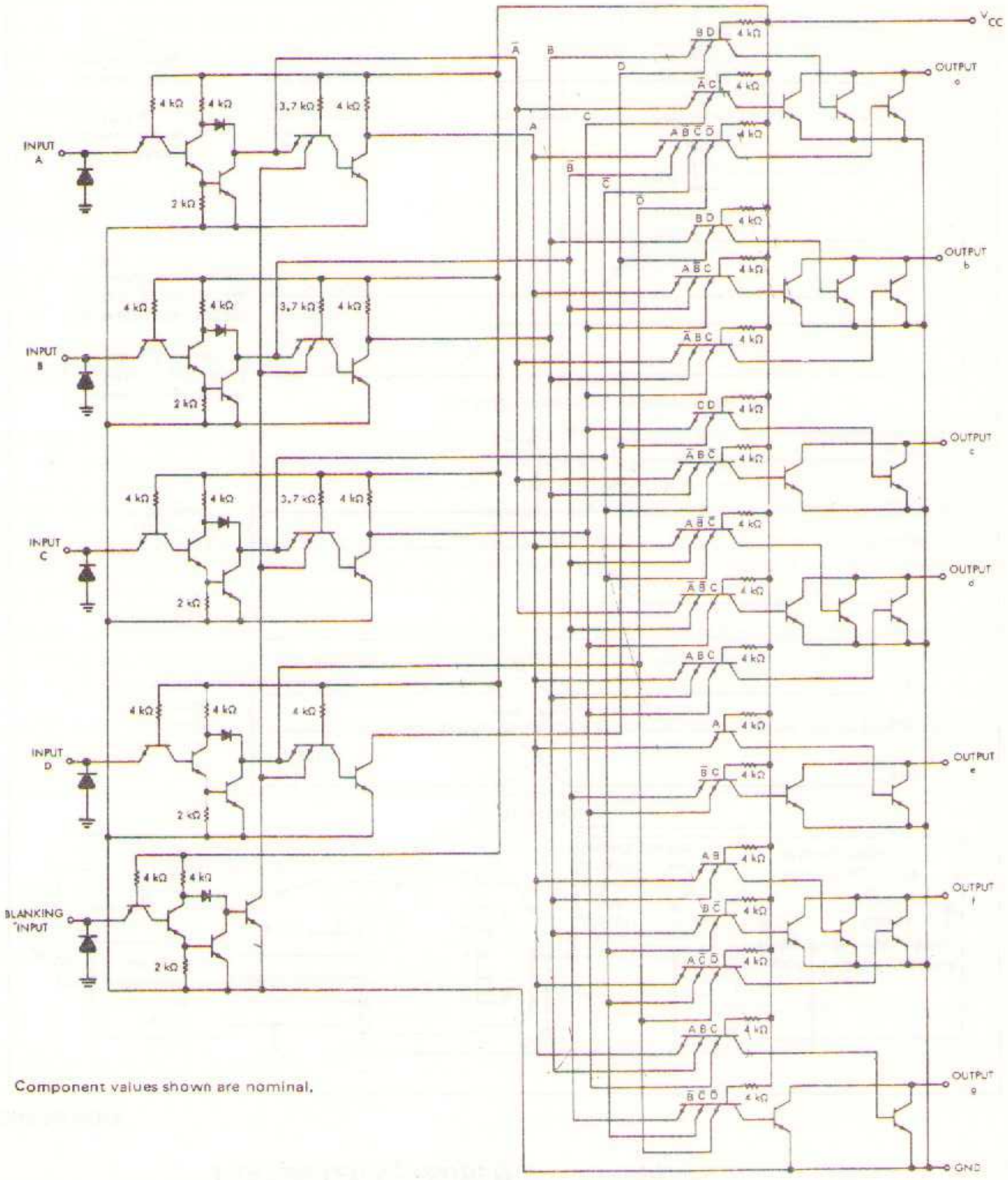


Component values shown are nominal

functional block diagram



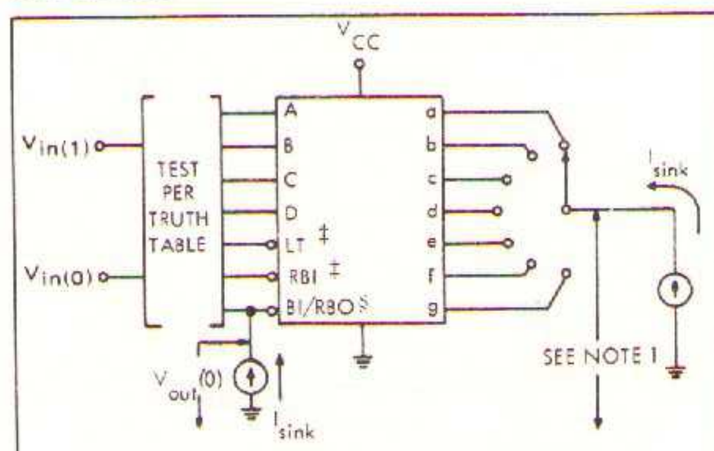
schematic diagram



Component values shown are nominal.

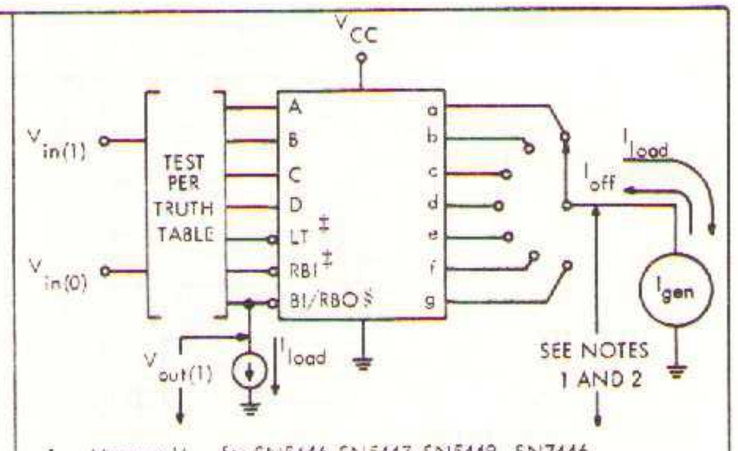
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



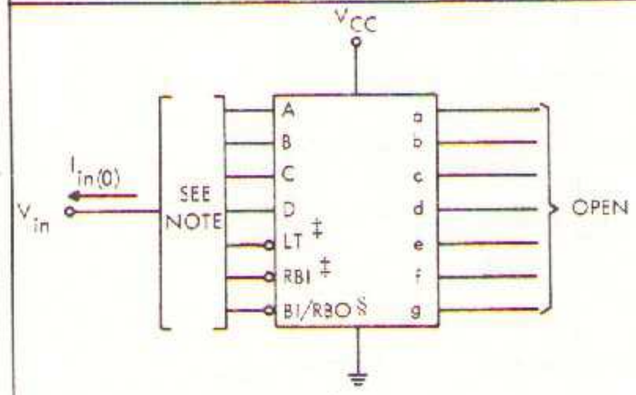
1. Measure V_{on} for SN5446, SN5447, SN5449, SN7446, SN7447, and SN7449. Measure $V_{out(0)}$ for SN5448 and SN7448.

FIGURE 1



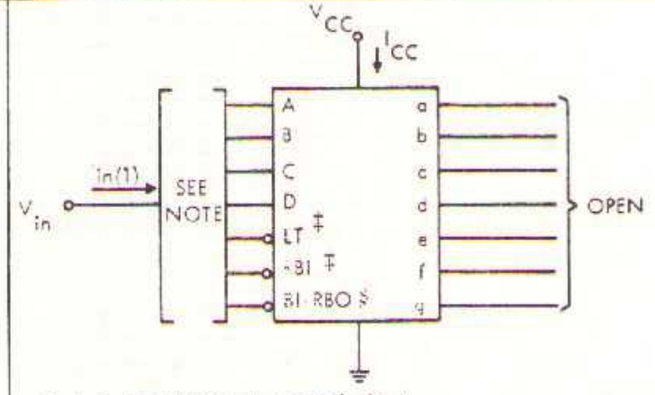
1. Measure V_{off} for SN5446, SN5447, SN5449, SN7446, SN7447, and SN7449.
2. Measure $V_{out(1)}$ for SN5448 and SN7448.

FIGURE 2



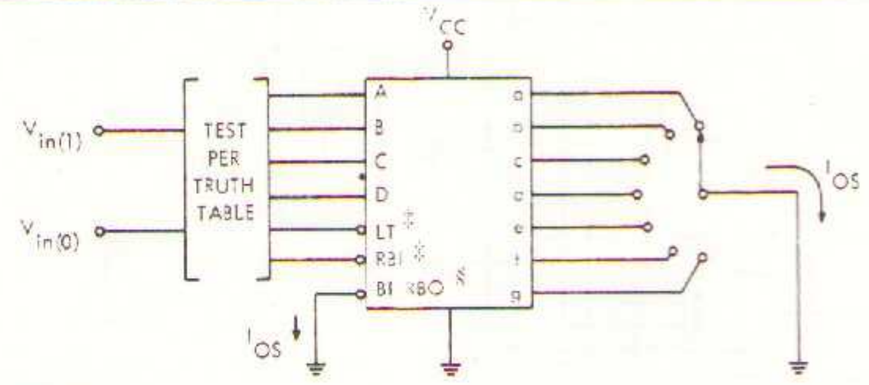
1. Each input is tested separately.

FIGURE 3



1. Each input is tested separately for $I_{in(1)}$.

FIGURE 4



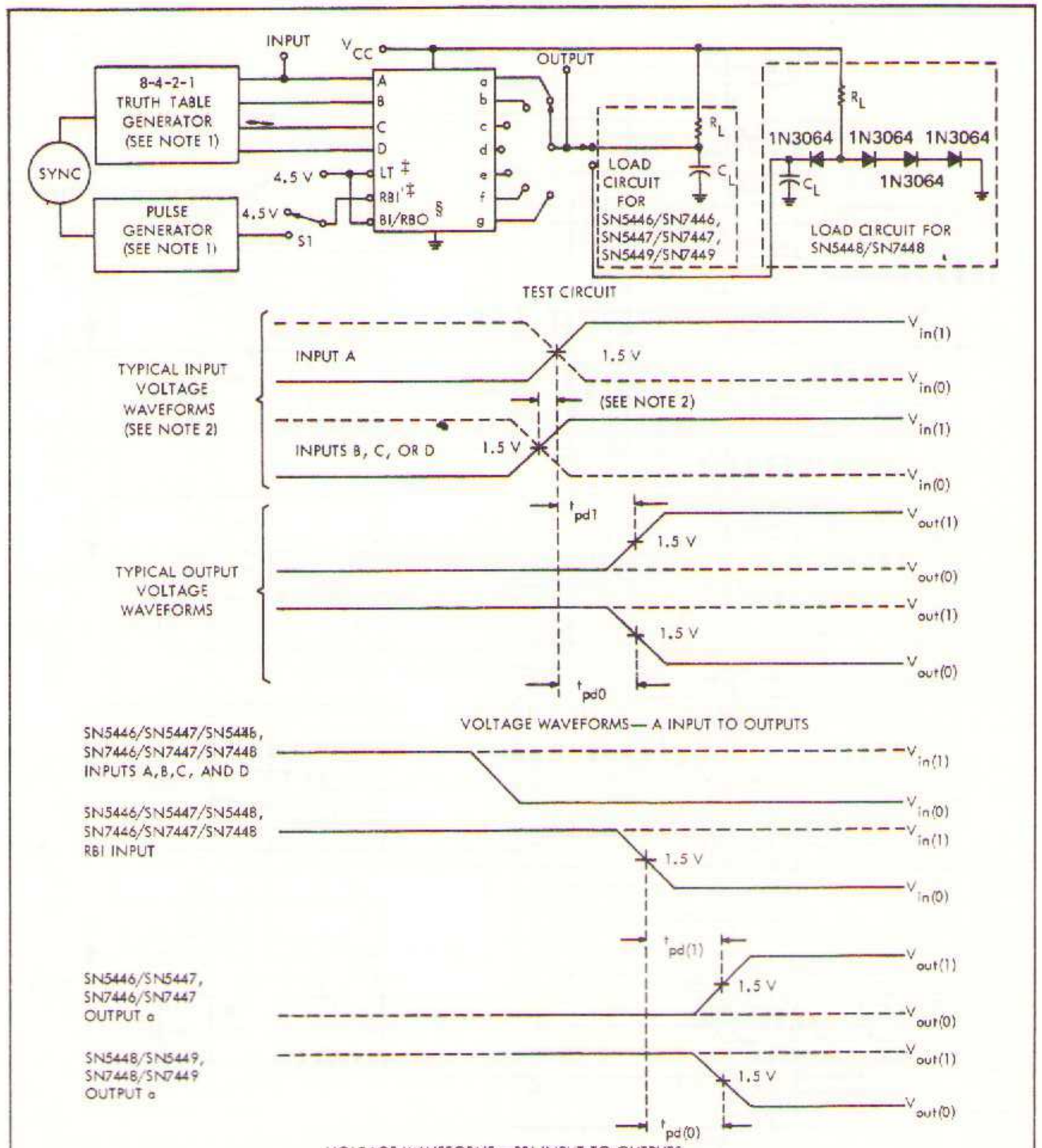
1. Each output is tested separately.

FIGURE 5

† Arrows indicate actual direction of current flow. Logic symbol used is representative for all types.
‡ Available on SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 only.
§ BI is available on all types. RBO node is available on SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 only.

PARAMETER MEASUREMENT INFORMATION

switching characteristics

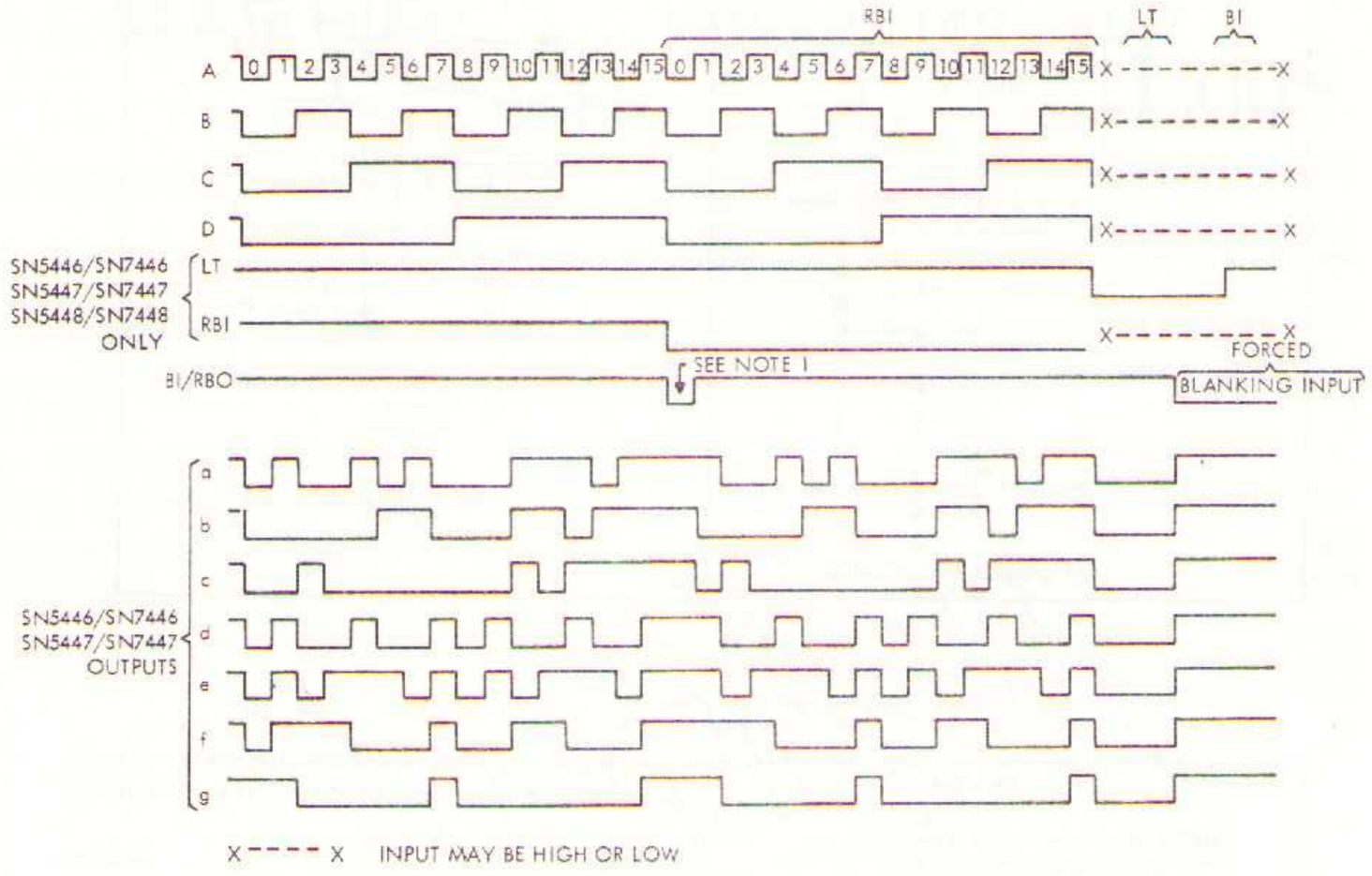


NOTES: 1. The truth table generator and pulse generator have the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f \leq 10$ ns, and PRR = 1 MHz.
2. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. RBI = 4.5 V.
3. C_L includes probe and jig capacitance.

‡ Available on SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 only.
§ BI is available on all types. RBO node is available on SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 only.

FIGURE 6—SWITCHING TIMES

TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS



NOTE 1: For the SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 this logical 0 represents the RBO response. For the SN5449 and SN7449 a logical 0 pulse is applied to the blanking input.

driving indicators directly (see Figure B)

This application demonstrates how the SN5446 or SN5447 may be used to drive seven-segment indicators directly. The output transistors of these two circuit types will sink up to 20 milliamperes of current; therefore, external components are not required.

Also illustrated is how the quacruple latch (SN5475) and decade counter (SN5490) may be utilized to acquire and store the numeral to be displayed. The method shown is typical of a single stage and a number of methods are possible for distributing the BCD data from the decade counter to the quadruple latch.

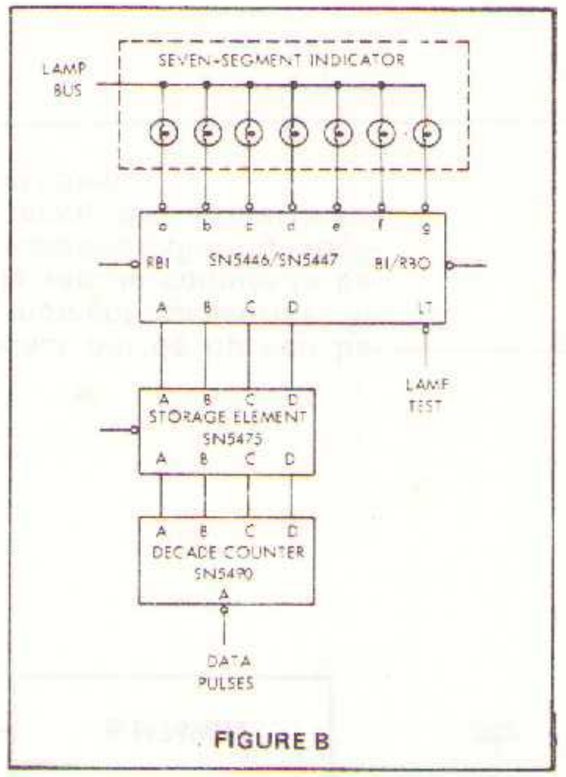


FIGURE B

n-digit display with leading-and trailing-edge blanking (see Figure C)

This application demonstrates a method for driving incandescent, seven-segment, display indicators directly from the output of the SN5446, or SN5447 decoder with provisions for leading-edge and trailing-edge zero-blanking, intensity control, and lamp test.

Leading-edge and trailing-edge zero blanking is illustrated for a six-digit mixed integer with zero indications suppressed for the two most-significant decades (MSD) of the whole number and the two least-significant decades (LSD). This scheme causes the number to be displayed in its easily identified, common form. Blanking is accomplished by grounding RBI inputs of most-significant and least-significant decades and interconnecting the BI/BRO nodes of these two decades to the ripple-blanking inputs of the adjacent decades. This improves readability by inhibiting suppression of zeros occurring on either side of the decimal point. The ripple-blanking inputs of the decades on either side of the fixed decimal point are inhibitec by connecting to a 5-volt d-c source.

Intensity control is accomplished at all six of the decoder/drivers by modulating the blanking input with a nultivibrator. Best results are obtained with a modulation source in which the duty cycle can be varied. Individual drivers are required as they are wire-OR connected with the ripple-blanking functions.

As the lamp-test input is only one load, a number (up to ten) of these may be driven from a single Series 54/74 circuit.

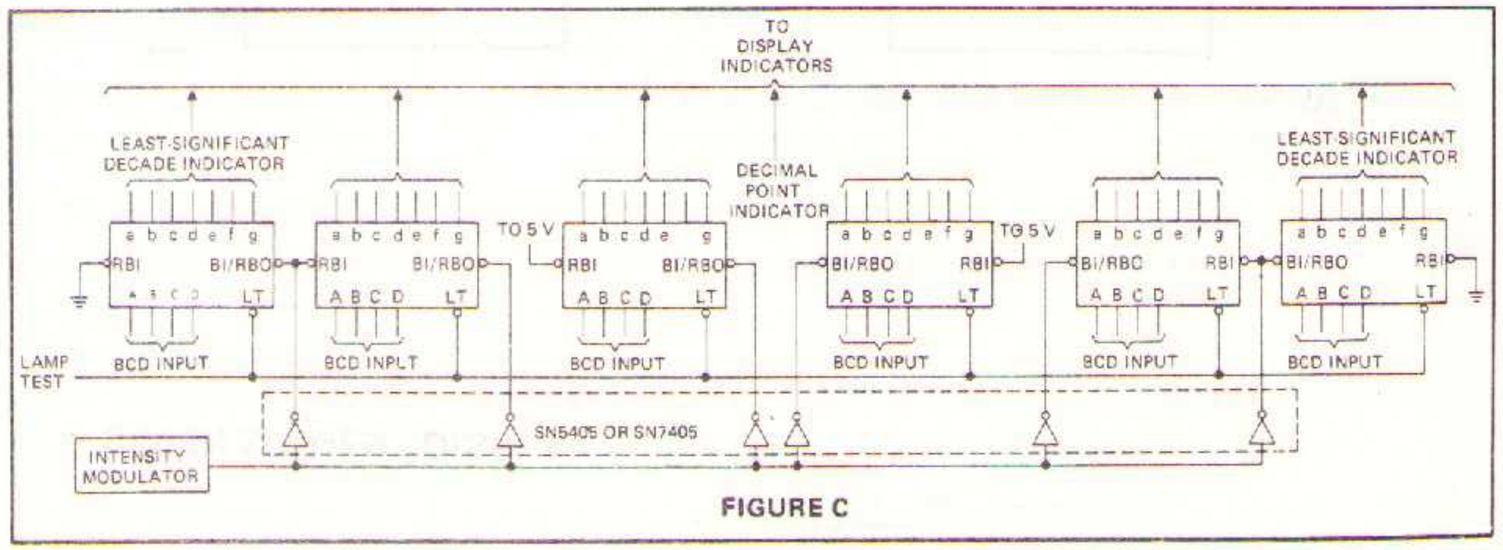


FIGURE C

APPLICATIONS DATA

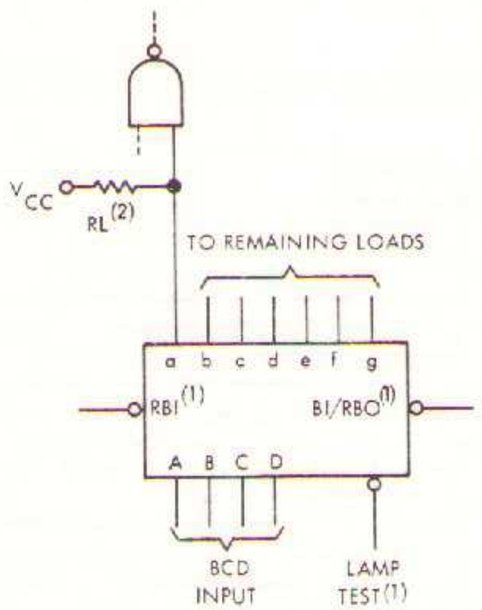
driving logic circuits (see Figure D)

These decoder/drivers may be used to drive other logic circuits. (See Figure D.) Value of the pull-up resistor (required on the open-collector outputs) may be calculated using the methods given for the SN5401 open-collector NAND gate.

driving buffer transistors (see Figures E and F)

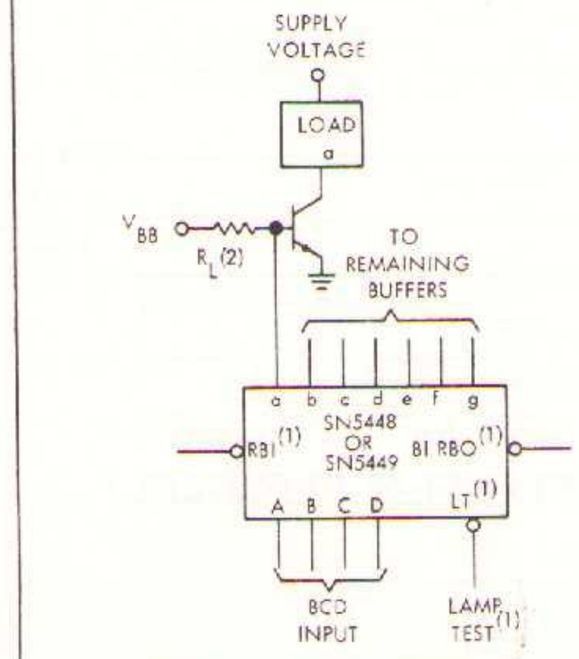
For applications requiring increased drive currents these decoder/drivers may be used with discrete drivers. A universal method of supplying base drive for a buffer transistor is illustrated in Figure E. Value of the base resistor (required on the open-collector outputs) may be calculated using the methods similar to those given for the SN5401 open-collector NAND gate. Increased base drive from the SN5448 is possible with the employment of external base resistor.

Circuitry for employing SCR's to drive electro-luminescent displays is illustrated in Figure F.



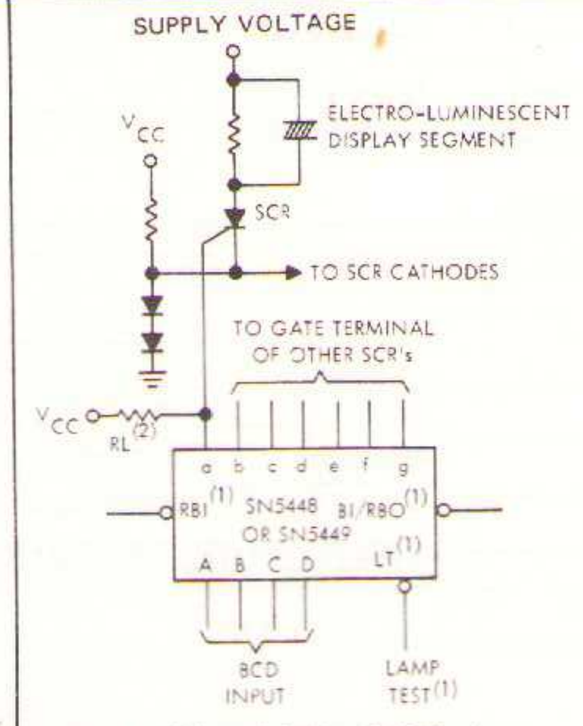
1. Available on SN5446, SN5447, SN5448, SN7446, SN7447, and SN7448 only.
2. Pull-up resistor is required with SN5446, SN5447, SN5449, SN7446, SN7447 or SN7449, and is optional with SN5448 or SN7448.

FIGURE D



1. Available on SN5448 and SN7448 only.
2. Pull-up resistor is required with SN5449 or SN7449, and is optional with SN5448 or SN7448.

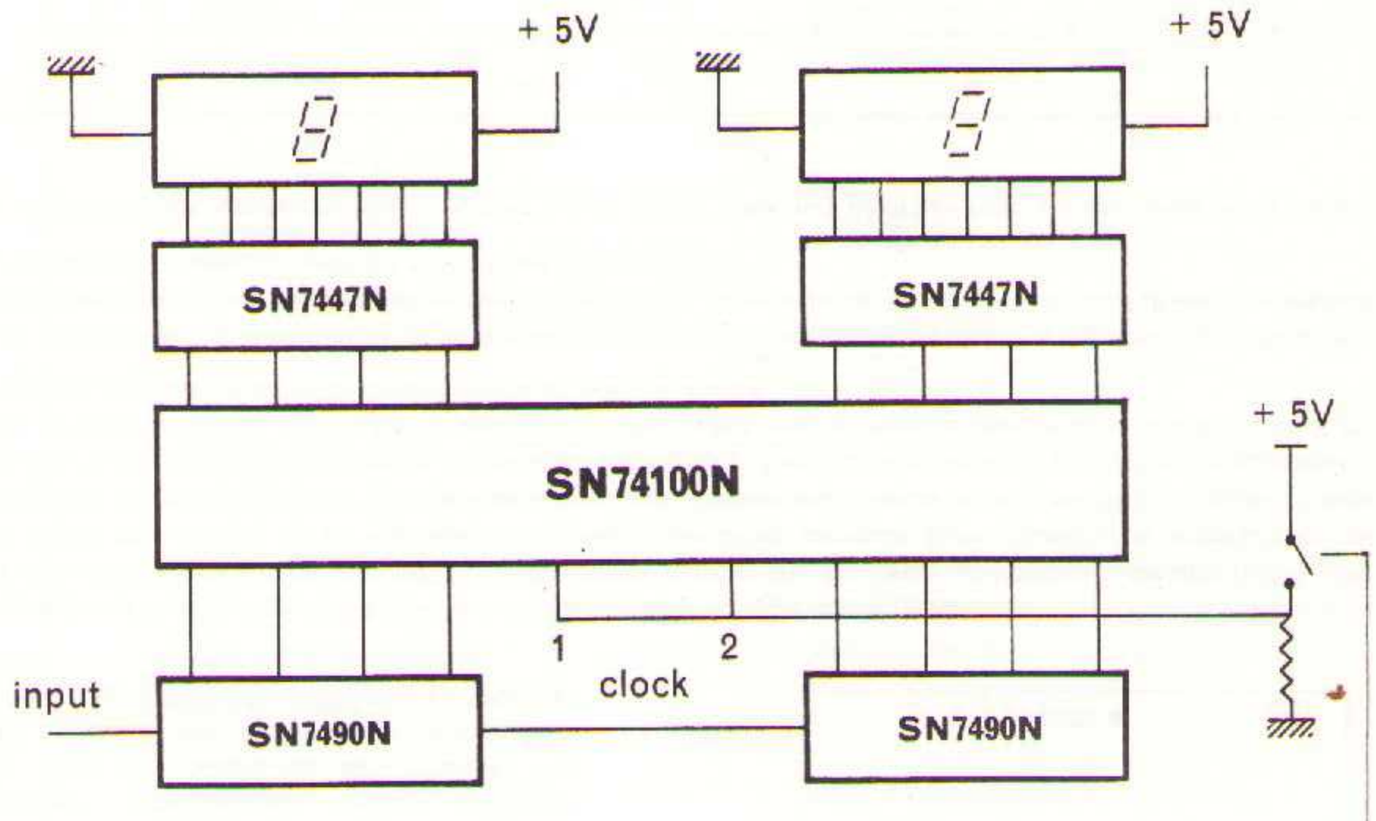
FIGURE E



1. Available on SN5448 and SN7448 only.
2. Pull-up resistor is required with SN5449 or SN7449, and is optional with SN5448 or SN7448.

FIGURE F

SEVEN SIGMENT DISPLAY



Schakelaar om de op een bepaald moment aanwezige informatie van de counter te bewaren waardoor aflezing mogelijk is, terwijl de counter doorgaat met tellen.

Nieuw

Voltage regulator L005

STANDARD TEMPERATURE RANGE, 0°C÷70°C

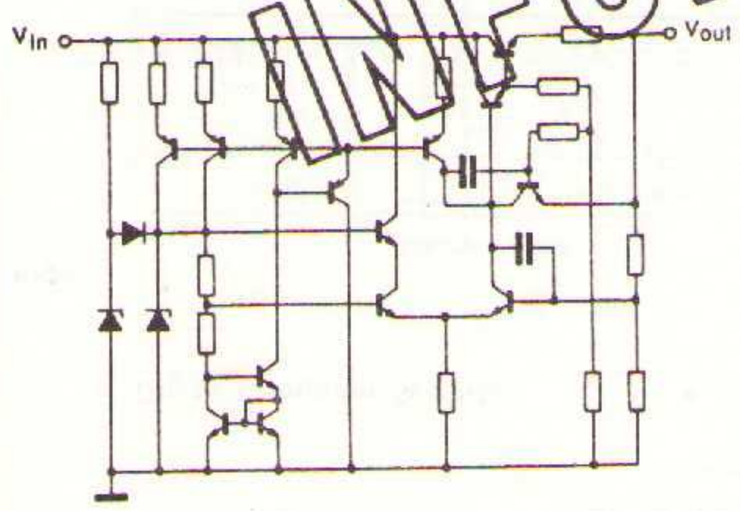
- OUTPUT CURRENT > 600 mA
- TIGHT TOLERANCE FOR OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 62 dB TYPICAL
- OVERLOAD AND SHORT CIRCUIT PROTECTION

The L 005 T1 is a monolithic 5V voltage regulator which can supply more than 600 mA.
The device features high temperature stability, internal overload and short circuit protection, low output impedance and excellent transient response.
The L 005 T1 is intended for use as voltage supply for digital circuits and for any other industrial application.

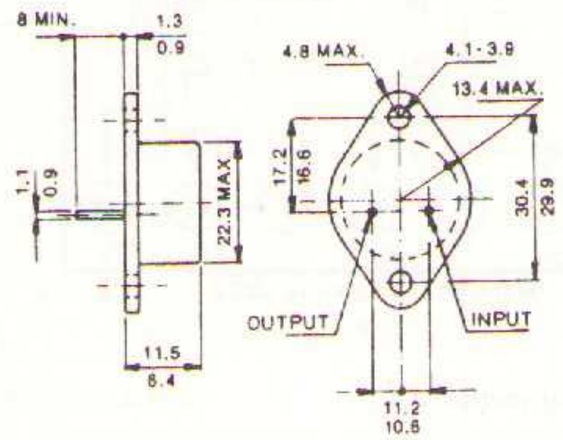
ABSOLUTE MAXIMUM RATINGS

Input Voltage	20V
Power Dissipation (free air, T_A = 25°C)	3.25W
Power Dissipation (with infinite heat sink, T_C = 25°C)	12.75W
Storage Temperature Range	−55°C ÷ 175°C
Operating Temperature Range	0°C to + 70°C

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
In accordance with
JEDEC TO - 3 outline



Notes
All dimensions in mm
Leads 1 and 2 electrically isolated from case.
Case is third electrical connection (ground).
Leads are gold-plated nickel-alloy.

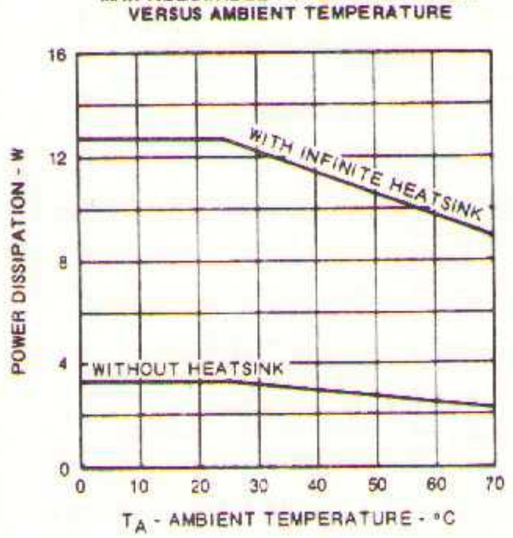
ORDERING NUMBER
L005 T1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

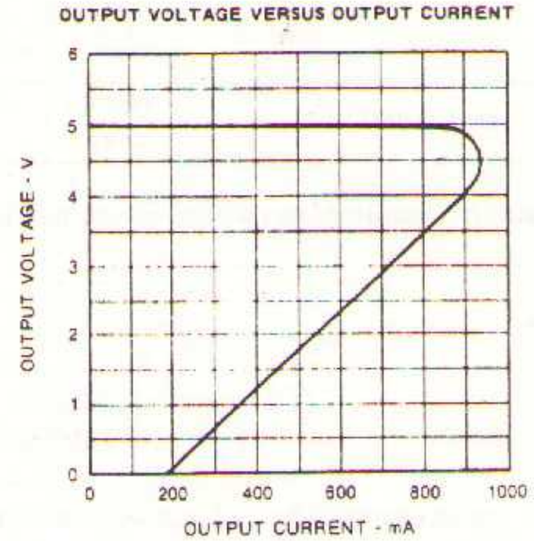
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Output Voltage	V_{in} = 7.5V ÷ 20V, C_L = 10 μF, I_L = 10 mA	4.75	5.0	5.25	V
Load Regulation	V_{in} = 12V, I_L = 0 ÷ 600 mA		0.3	1	% Vout
Regulated Output Current	V_{in} = 12V, $\frac{\Delta Vout}{Vout} \leq 1\%$	600	850		mA
Maximum Output Current	V_{in} = 12V		930	1200	mA
Output Resistance	V_{in} = 12V, I_L = 0.6A		15		mΩ
Line Regulation	V_{in} = 7.5V ÷ 12V, C_L = 10 μF, I_L = 10 mA		0.1	0.5	% Vout
Ripple Rejection	V_{in} = 10V, ΔV_{in} = 4V_{pp}, f = 100 Hz	46	62		dB
Output Noise Voltage	V_{in} = 12V, I_L = 10 mA, C_L = 20 μF BW = 10 Hz ÷ 100 KHz		0.07		mV
Standby Current	V_{in} = 20V, I_L = 0		9		mA
Temperature Coefficient	V_{in} = 12V, I_L = 10 mA, C_L = 10 μF T_A = 0°C ÷ 60°C		0.003		%/°C
Short Circuit Current	V_{in} = 12V, V_{out} = 0		190	250	mA

TYPICAL ELECTRICAL CHARACTERISTICS

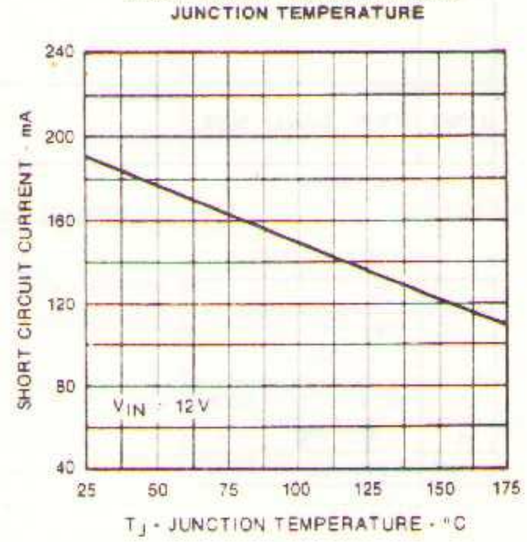
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



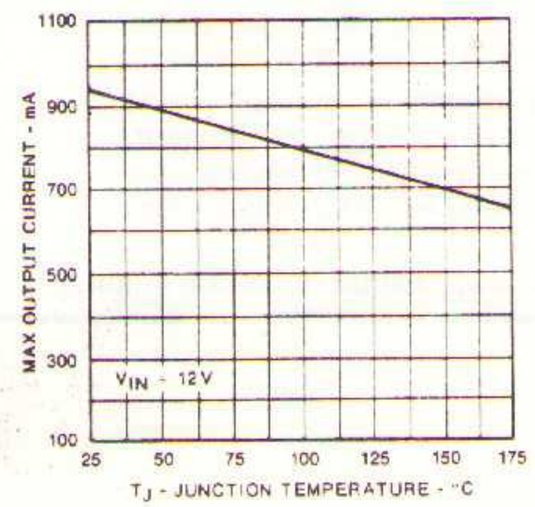
OUTPUT VOLTAGE VERSUS OUTPUT CURRENT



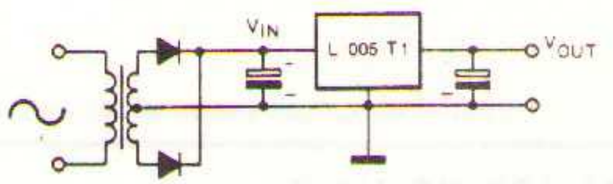
SHORT CIRCUIT CURRENT VERSUS JUNCTION TEMPERATURE



MAX OUTPUT CURRENT VERSUS JUNCTION TEMPERATURE



TYPICAL APPLICATION CIRCUIT



A HIGH-SPEED TTL 2-BIT FULL ADDER
FOR APPLICATION IN

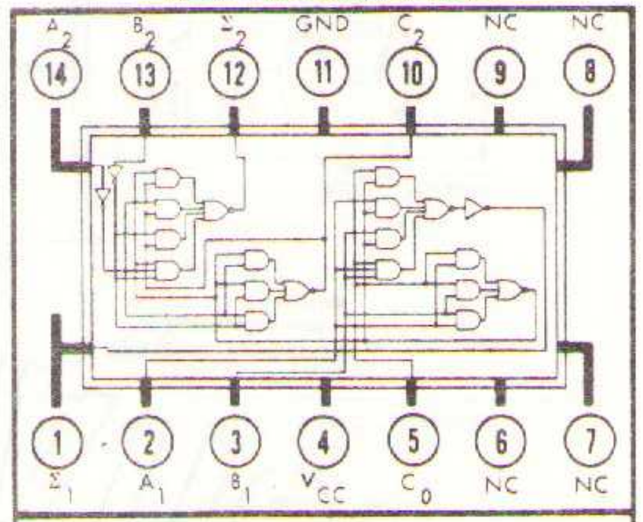
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

TRUTH TABLE

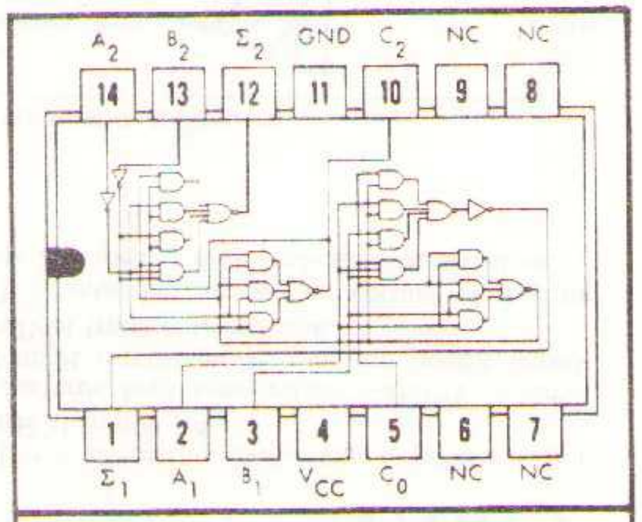
INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

S
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

description

This full adder performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 V
Operating Case Temperature Range: SN5482S	−55°C to 125°C
Operating Free-Air Temperature Range: SN5482J, SN5482N	−55°C to 125°C
SN7482 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5482 Circuits	4.5	5	5.5	V
SN7482 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:				
C_2			5	
Σ_1 or Σ_2			10	

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN				0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current at Σ_1 or Σ_2§	4	V_{CC} = MAX	SN5482	−20		−55	mA
				SN7482	−18		−55	mA
I_{OS}	Short-circuit output current at C_2§	4	V_{CC} = MAX	SN5482	−20		−70	mA
				SN7482	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX	SN5482		35	50	mA
				SN7482		35	58	mA

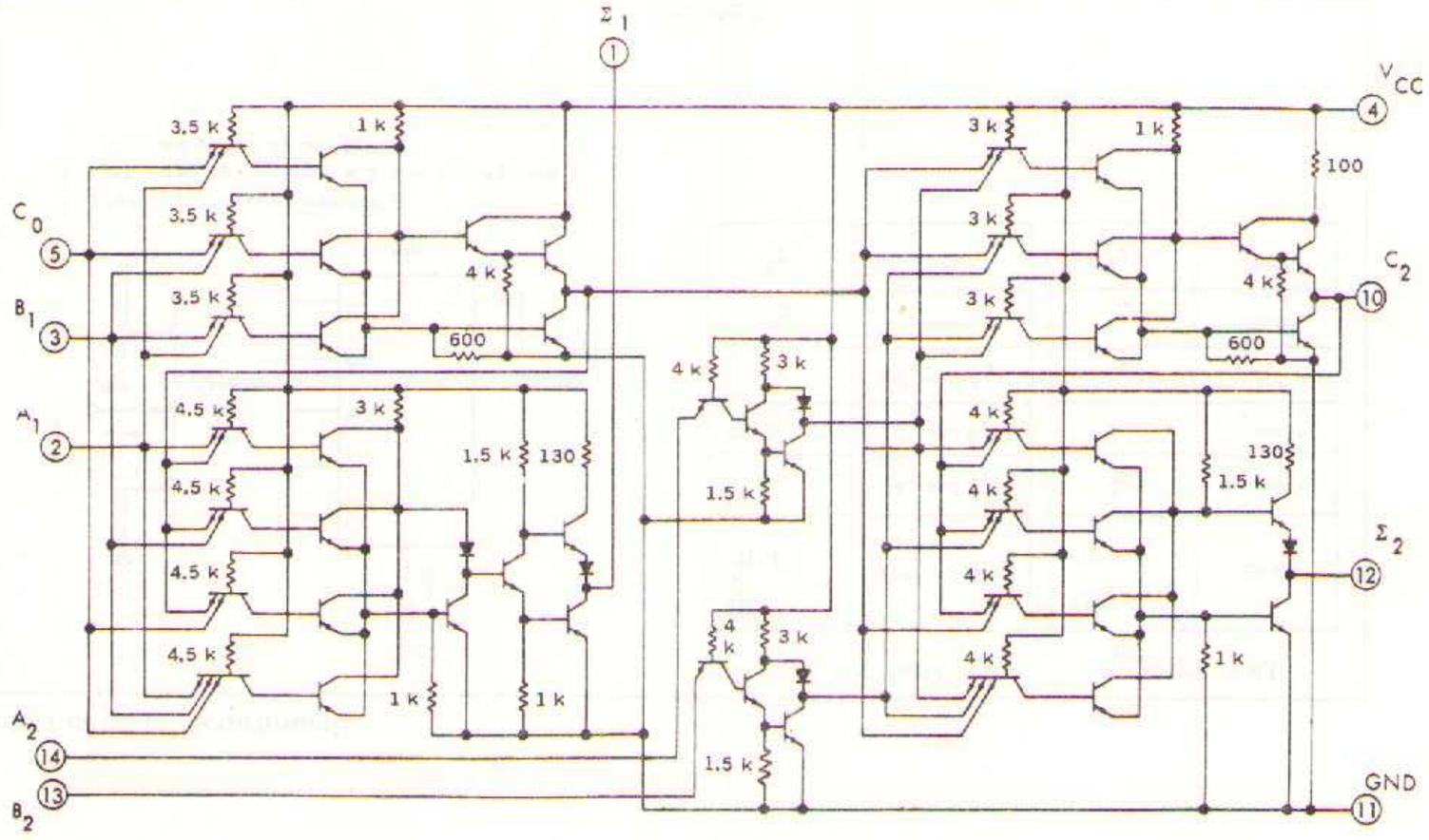
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	Σ_1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	B_2	Σ_2	3	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	C_0	Σ_2	5	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	C_2	7	C_L = 15 pF, R_L = 400 Ω		17	27	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω		12	19	ns

§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

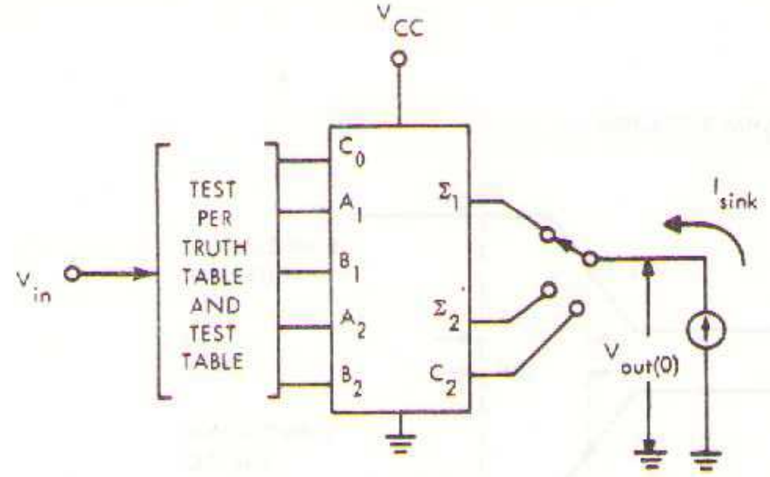
schematic



Component values shown are nominal.
Resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

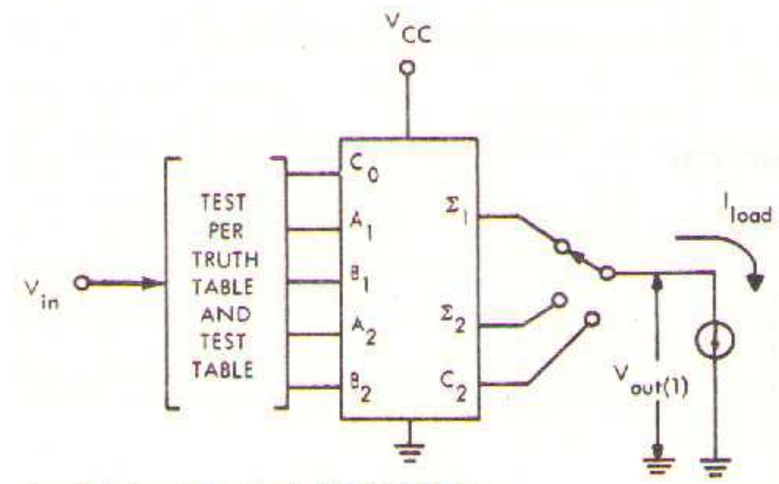


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1 or Σ_2	16 mA
C_2	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

OUTPUT UNDER TEST	I_{load}
Σ_1 or Σ_2	−400 μA
C_2	−200 μA

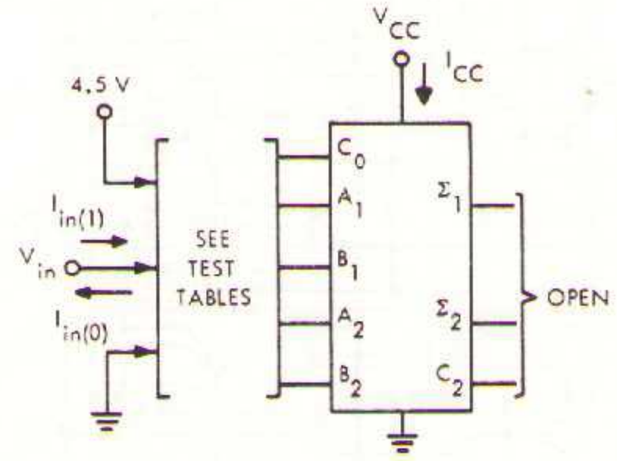
1. Each input or output is tested separately.

FIGURE 2

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



$I_{in(0)}$ TEST TABLE

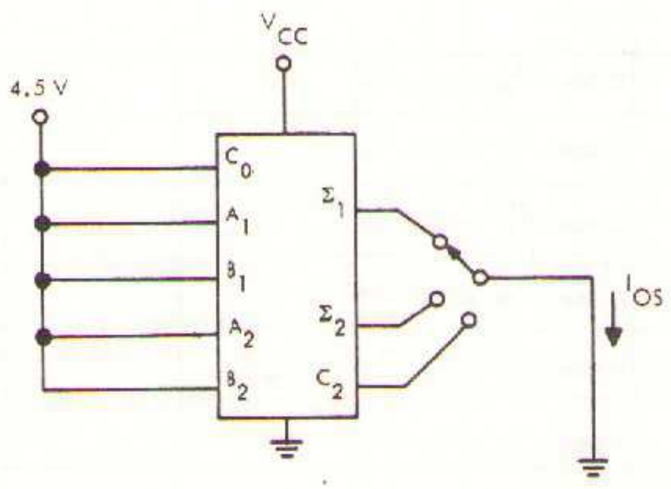
APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, and C_0; and ground B_1 and B_2.

FIGURE 3

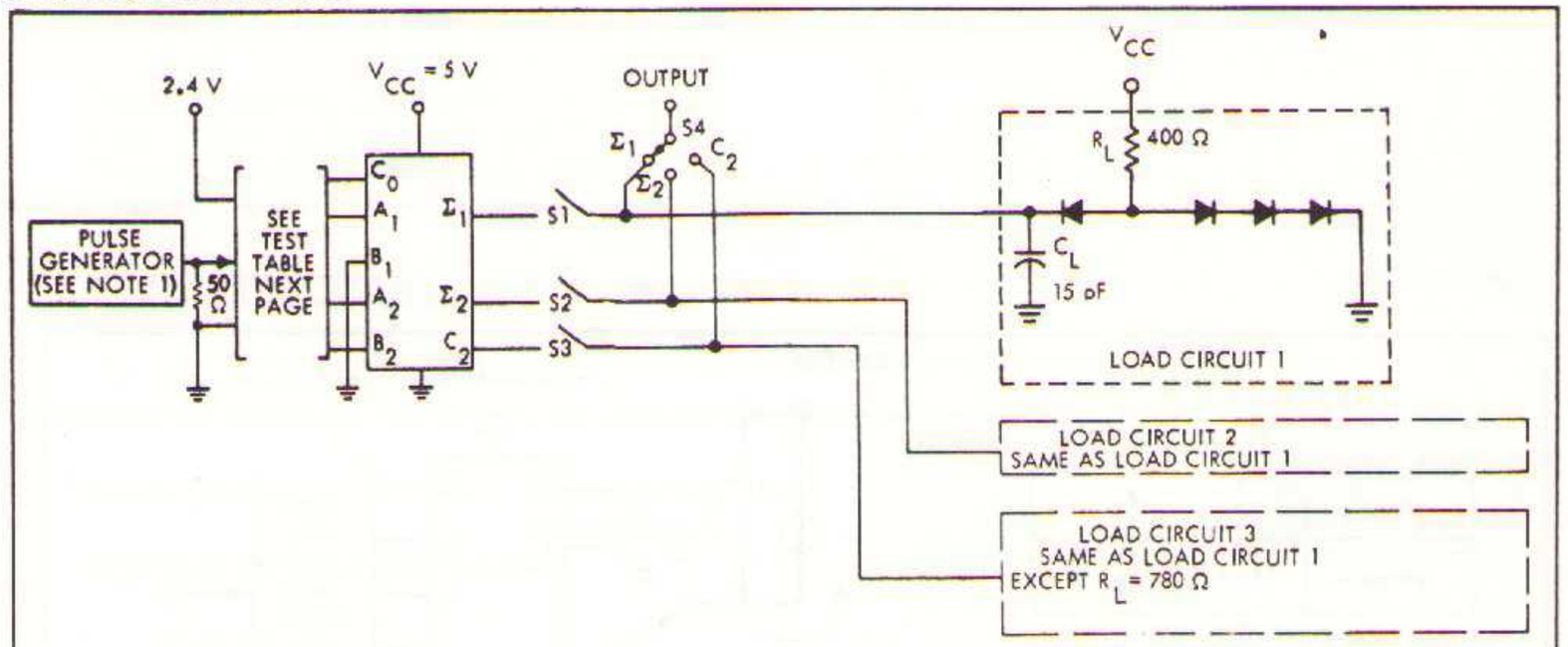


1. Each output is tested separately.

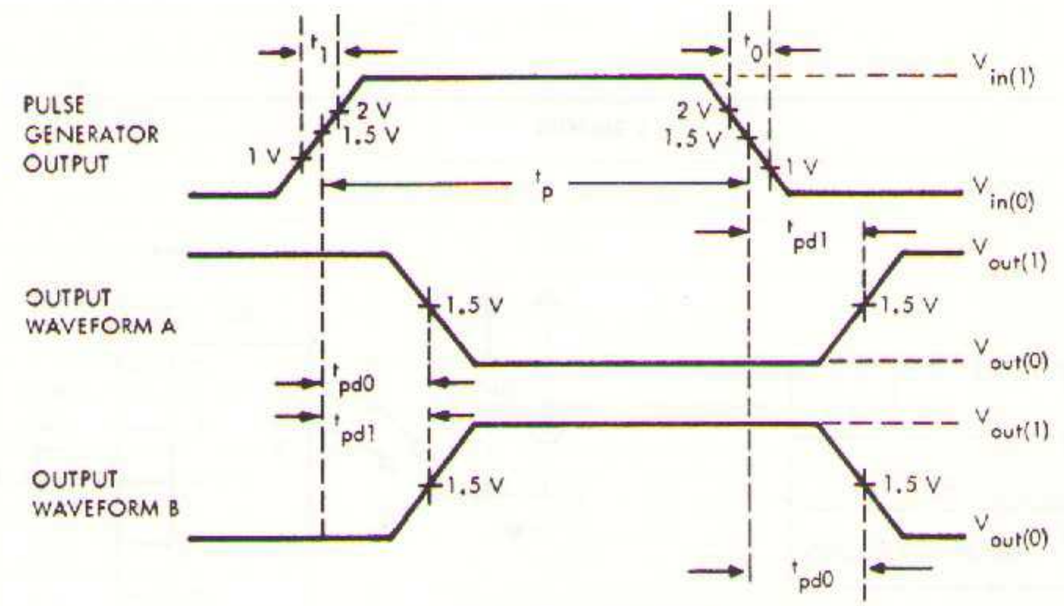
FIGURE 4

†Arrows indicate actual direction of current flow.

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: $V_{in(1)} \geq 2.4$ V, $V_{in(0)} \leq 0.4$ V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 5–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

SWITCHING TIMES TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S4)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	A_2, B_1, B_2	CLOSED	OPEN	OPEN
2	t_{pd0}							
3	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2 and C_0	OPEN	CLOSED	OPEN
4	t_{pd0}							
5	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1, A_2	B_1, B_2	OPEN	CLOSED	CLOSED
6	t_{pd0}							
7	t_{pd1}	C_0	C_2 (WAVEFORM B)	A_1, A_2	B_1, B_2	OPEN	OPEN	CLOSED
8	t_{pd0}							

NOTE 7: Inputs and outputs not otherwise specified are open.

I N D I C A T I E B U I Z E N

Technische gegevens van de bij deze geïntegreerde schakelingen toe te passen cijferindicatiebuizen zijn opgenomen in onze uitgave:

Technische documentatie deel 5-6 pagina 69 t/m 73 (ZM1000 - ZM1024)

Technische documentatie deel 7-9 pagina 2 t/m 3 (7-segmentbuis DG12H)

Nieuw in ons leveringsprogramma zijn de 7 segment LED systemen van Texas Instruments; hiervan is het dual-in-line type TIXL 302 uit voorraad leverbaar. De stuksprijs bedraagt *f* 74,- excl. 14% B.T.W.

HIGH-SPEED TTL 4-BIT FULL ADDERS
FOR APPLICATION IN

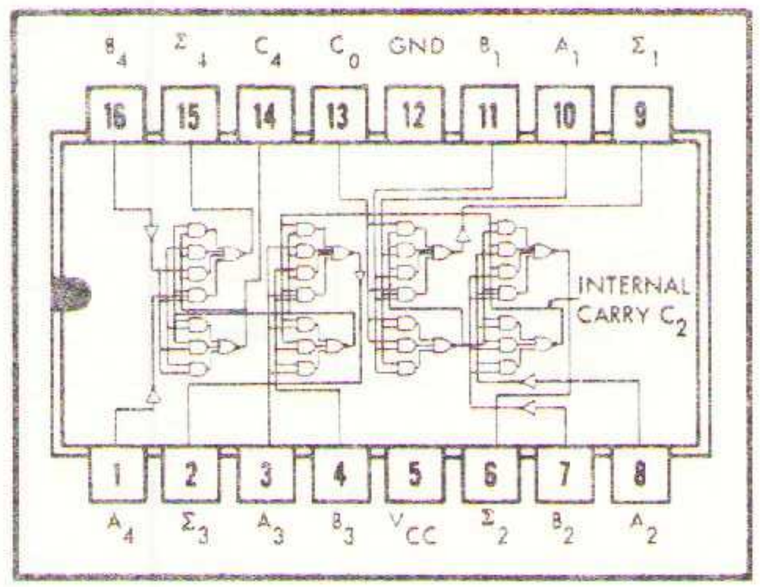
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
				WHEN $C_2 = 0$			WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5483 Circuits . . . . . −55°C to 125°C
SN7483 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: (See Note 1)	SN5483 Circuits	4.5	5	5.5	V
	SN7483 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:					
C_4				5	
Σ_1, Σ_2, Σ_3 or Σ_4				10	

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN				0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 0.4 V			−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 2.4 V			160	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at Σ_1, Σ_2, Σ_3, or Σ_4§	4	V_{CC} = MAX	SN 5483	−20		−55	mA
				SN7483	−18		−55	mA
I_{OS}	Short-circuit output current at C_4§	4	V_{CC} = MAX	SN5483	−20		−70	mA
				SN7483	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX,	SN5483		78	110	mA
				SN7483		78	128	mA

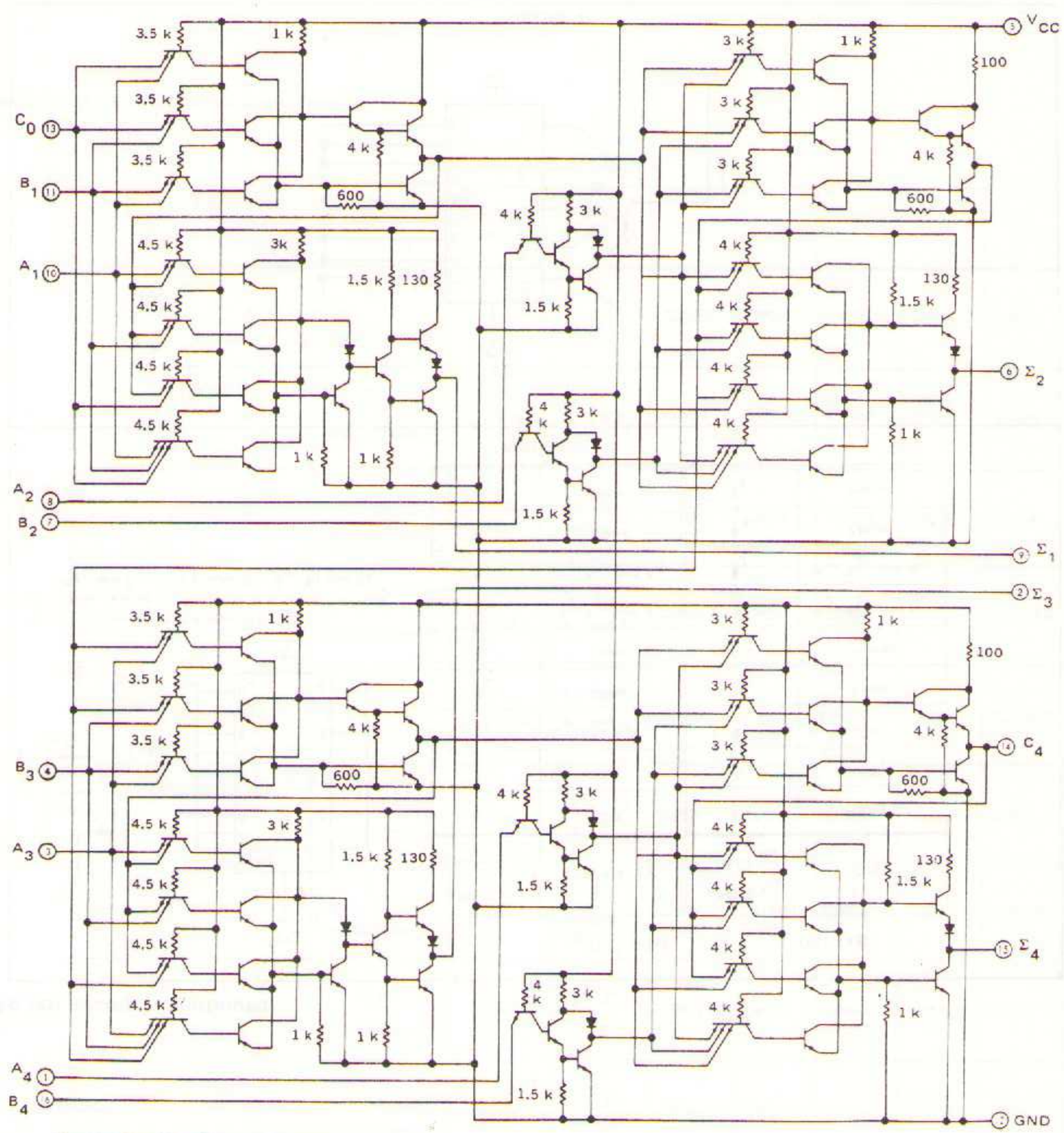
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteri tics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	C_0	2	3	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	3	5	C_L = 15 pF, R_L = 400 Ω			50	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			60	ns
t_{pd1}	C_0	4	7	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd1}	C_0	C_4	9	C_L = 15 pF, R_L = 780 Ω	35		48	ns
t_{pd0}			10	C_L = 15 pF, R_L = 780 Ω	22		32	ns
t_{pd1}	A_2 or B_2	2	11 and 13	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			12 and 14	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	A_4 or B_4	4	15 and 17	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			16 and 18	C_L = 15 pF, R_L = 400 Ω			35	ns

§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

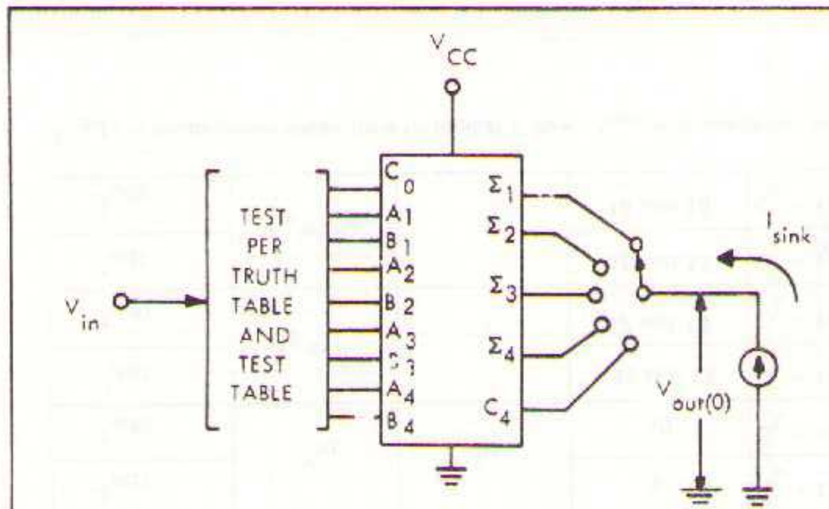
schematic



Component values shown are nominal.
Resistor values are in ohms.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

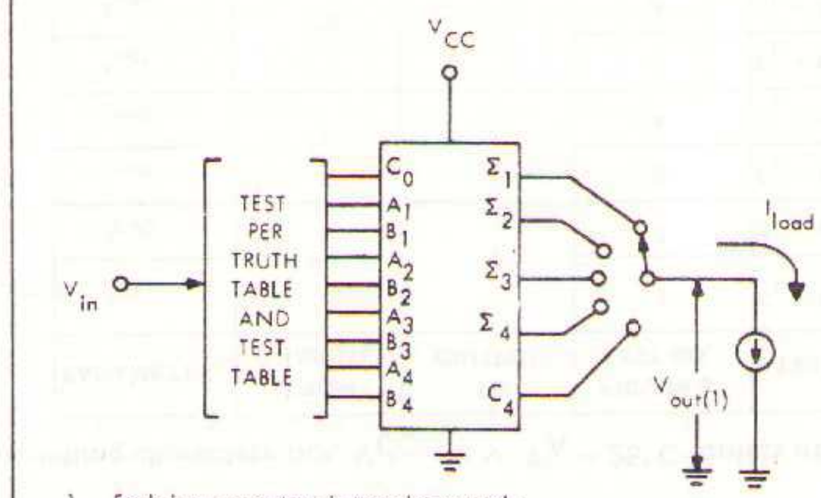


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1, Σ_2, Σ_3, or Σ_4	16 mA
C_4	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

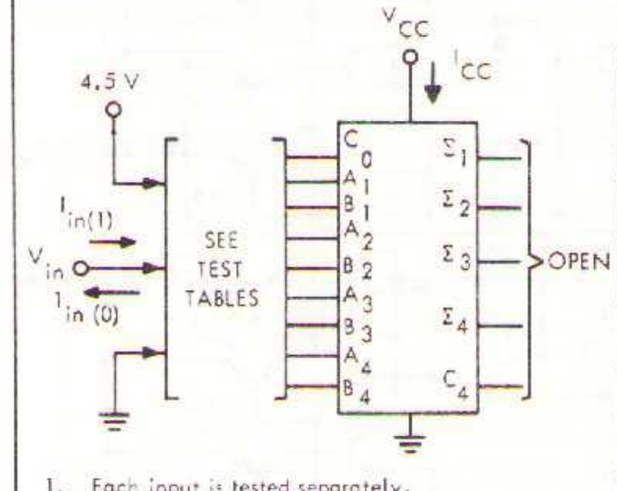
OUTPUT UNDER TEST	I_{load}
Σ_1, Σ_2, Σ_3, or Σ_4	− 400 μA
C_4	− 200 μA

1. Each input or output is tested separately.

FIGURE 2

†Arrows indicate actual direction of current flow.

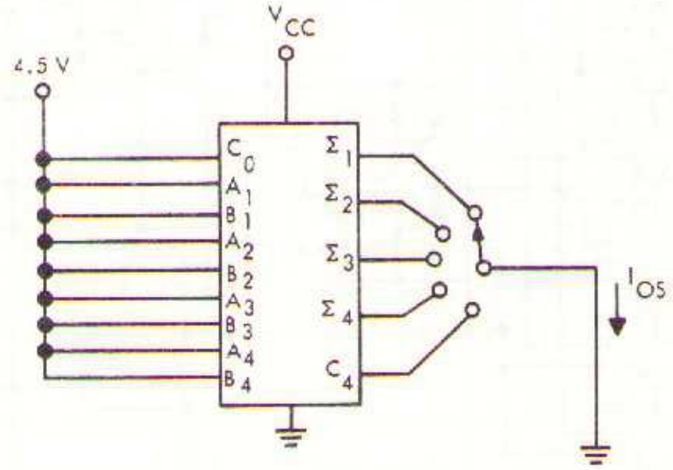
d-c test circuits† (continued)



1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, A_3, A_4, and C_0; and ground B_1, B_2, B_3 and B_4.

$I_{in(0)}$ TEST TABLE		$I_{in(1)}$ TEST TABLE	
APPLY V_{in} TEST I_{in}	APPLY 4.5 V	APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1	C_0	A_1 and B_1
A_1	C_0 and B_1	A_1	C_0 and B_1
B_1	C_0 and A_1	B_1	C_0 and A_1
A_2	None	A_2	None
B_2	None	B_2	None
A_3	A_2, B_2, and B_3	A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3	B_3	A_2, B_2, and A_3
A_4	None	A_4	None
B_4	None	B_4	None

FIGURE 3

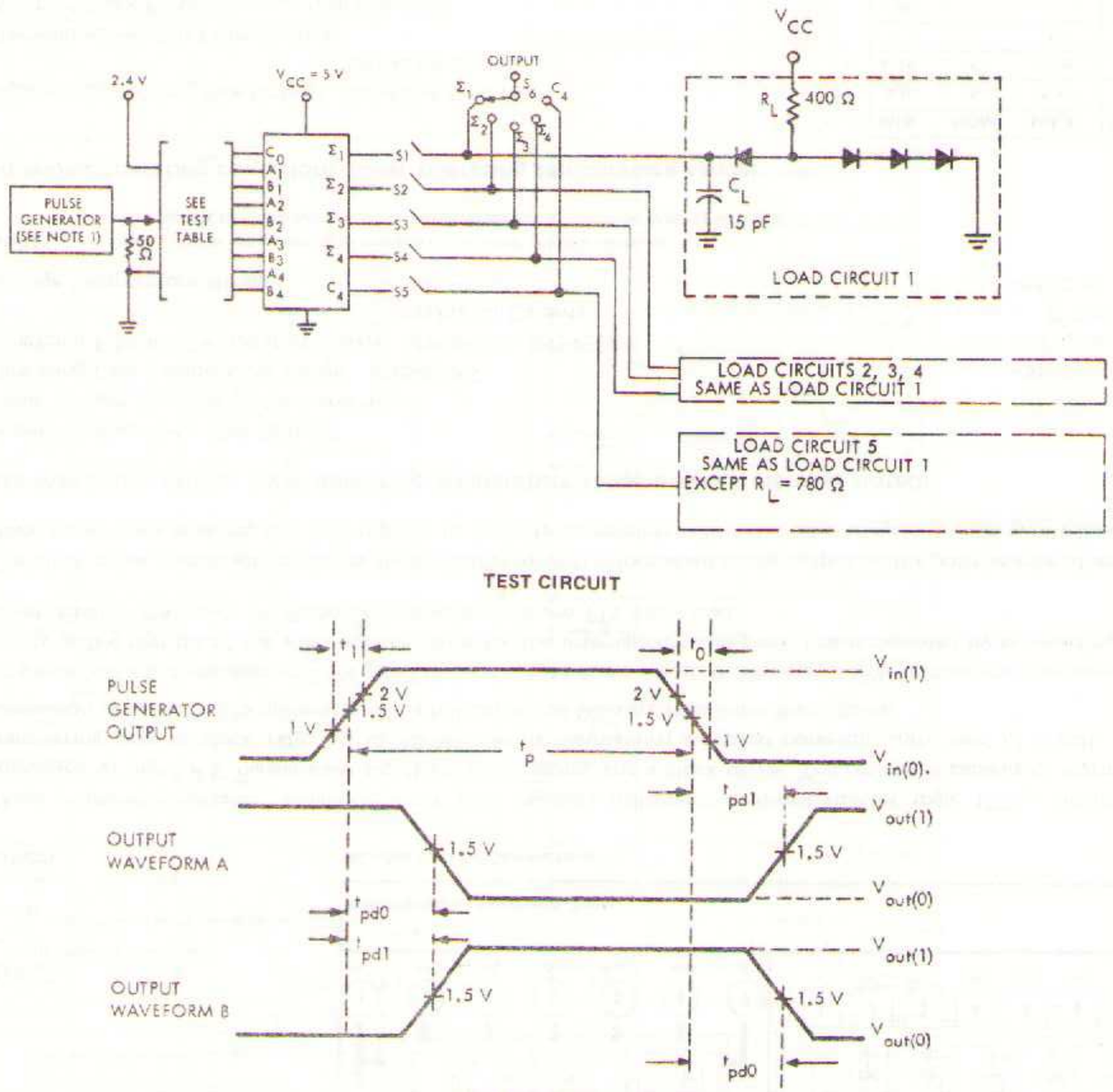


1. Each output is tested separately.

FIGURE 4

†Arrows indicate actual direction of current flow.

switching characteristics



NOTES: 1. Pulse generator output pulse characteristics: $V_{in(1)} \geq$ 2.4 V, $V_{in(0)} \leq$ 0.4 V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200 ns, and $Z_{out} \approx$ 50 Ω.

2. Perform test in accordance with test table. (See sheet 2 of this figure.)
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064

FIGURE 5–SWITCHING TIMES (SHEET 1 OF 2)

switching characteristics (continued)

TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	B_1, A_2, and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
2	t_{pd0}									
3	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
4	t_{pd0}									
5	t_{pd1}	C_0	Σ_3 (WAVEFORM A)	A_1, A_2, and A_3	B_1, B_2, and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
6	t_{pd0}									
7	t_{pd1}	C_0	Σ_4 (WAVEFORM A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
8	t_{pd0}									
9	t_{pd1}	C_0	C_4 (WAVEFORM B)	A_1, A_2, A3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
10	t_{pd0}									
11	t_{pd1}	A_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
12	t_{pd0}									
13	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
14	t_{pd0}									
15	t_{pd1}	A_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
16	t_{pd0}									
17	t_{pd1}	B_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN
18	t_{pd0}									

NOTE 7: Inputs and outputs not otherwise specified are open.

FIGURE 5 – SWITCHING TIMES (SHEET 2 of 2)

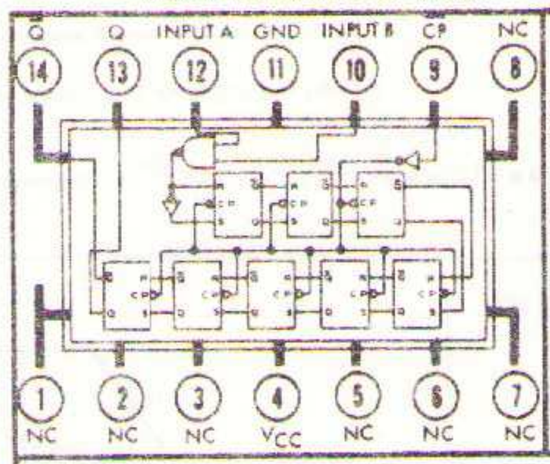
MSI TTL SHIFT REGISTERS

for applications in

• Digital Computer Systems • Data-Handling Systems • Control Systems

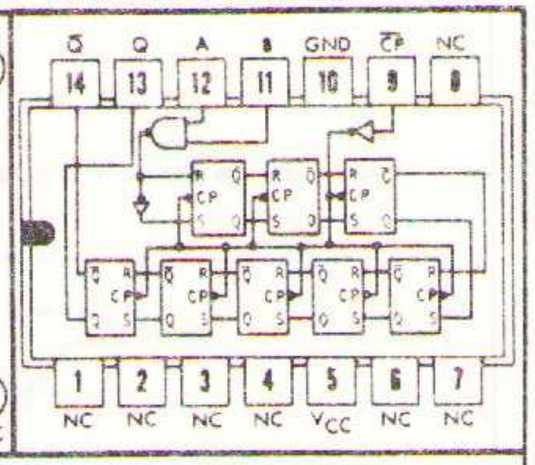
S

FLAT PACKAGE (TOP VIEW)



J OR N

DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See Truth Table

NC—No Internal Connection

logic

t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = bit time before clock.
2. t_{n+8} = bit time after 8 clock pulses.

description

These monolithic serial-in, serial-out, 8-bit shift registers utilizing transistor-transistor logic (TTL) circuits, are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and a full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with other edge-triggered synchronous functions.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Case Temperature Range: SN5491AS . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5491AJ, SN5491AN . . . . . −55°C to 125°C
SN7491A Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5491A Circuits	4.5	5	5.5	V
SN7491A Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 7)	25			ns
Input Setup Time, t_{setup} (See Figure 7)	25			ns
Input Hold Time, t_{hold} (See Figure 7)	0			

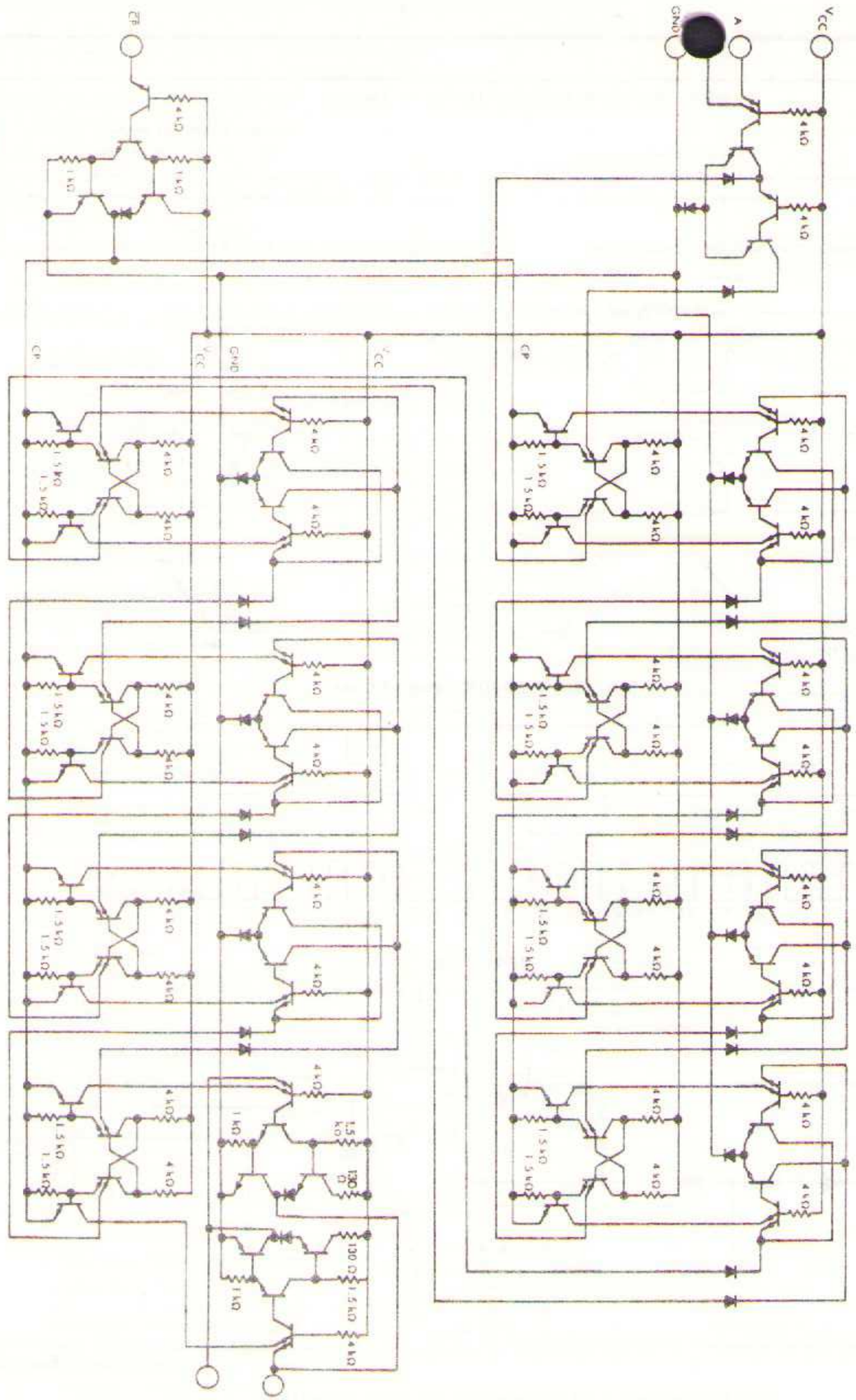
electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out} = 0	SN5491A	−20		−57	mA
				SN7491A	−18		−57	mA
I_{CC}	Supply current	6	V_{CC} = MAX, V_{in} = 4.5 V	SN5491A		35	50	mA
				SN7491A		35	58	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

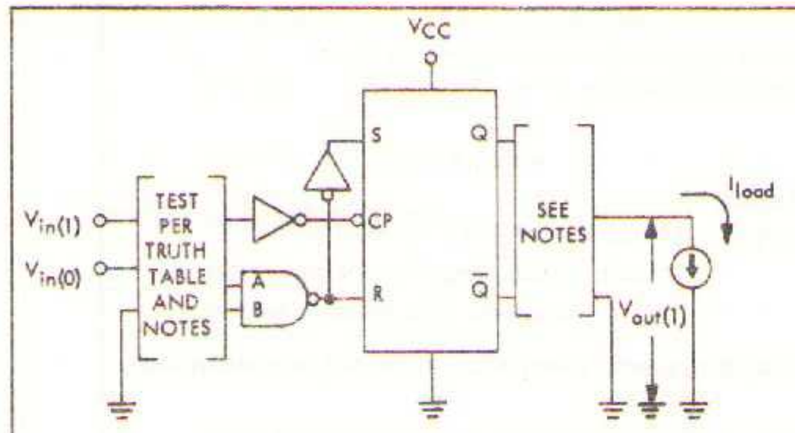
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	7	C_L = 15 pF, R_L = 400 Ω		24	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	7	C_L = 15 pF, R_L = 400 Ω		27	40	ns



Component values shown are nominal.

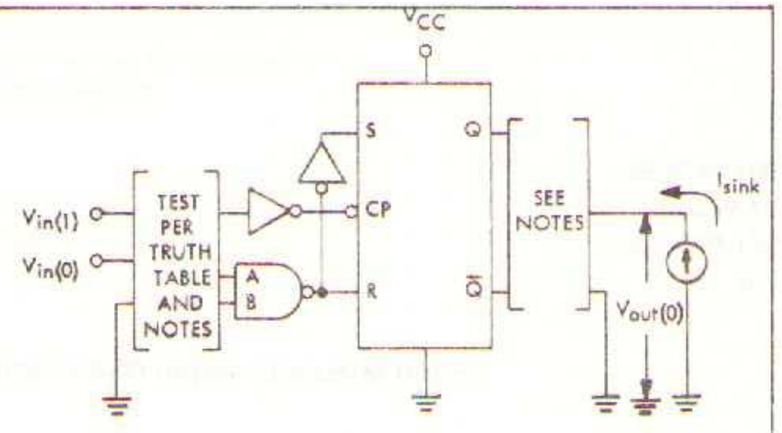
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



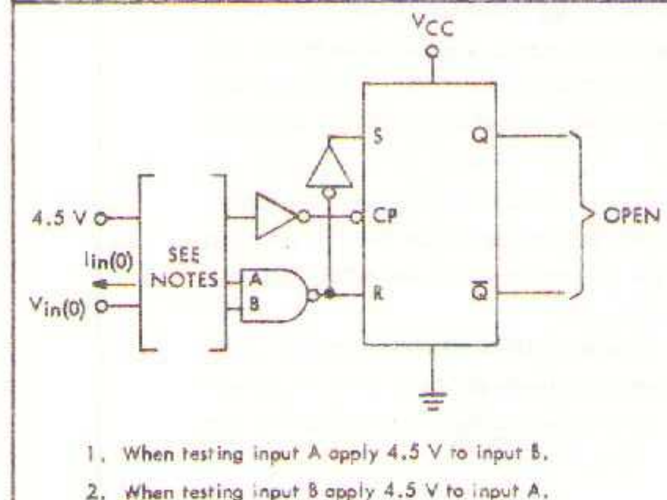
1. Each output is tested separately.
2. When testing $V_{out(1)}$ and I_{load}, ground all inputs and the unused output, then measure parameters specified.

FIGURE 1



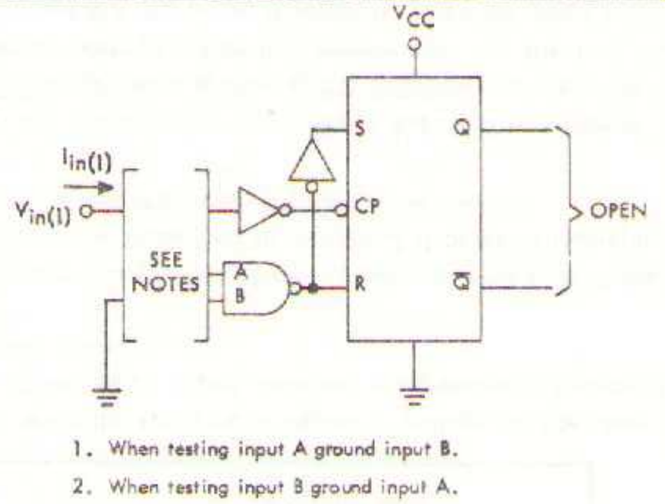
1. Each output is tested separately.
2. When testing $V_{out(0)}$ and I_{sink}, ground all inputs. Apply a momentary ground to the output to be tested then measure parameters specified.

FIGURE 2



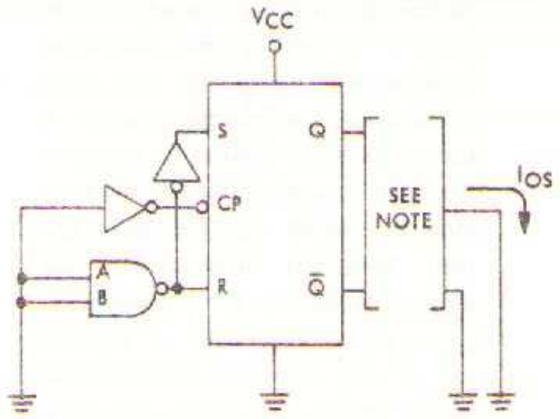
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

FIGURE 3



1. When testing input A ground input B.
2. When testing input B ground input A.

FIGURE 4



1. Ground the unused output then measure parameter specified.

FIGURE 5

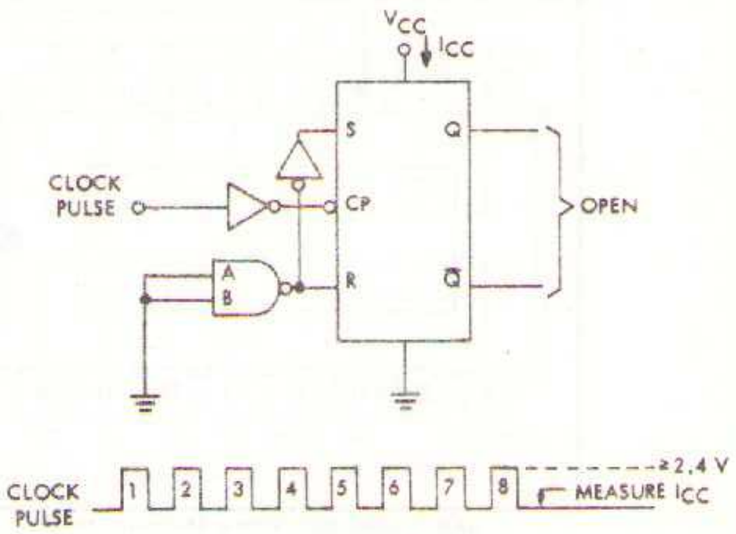
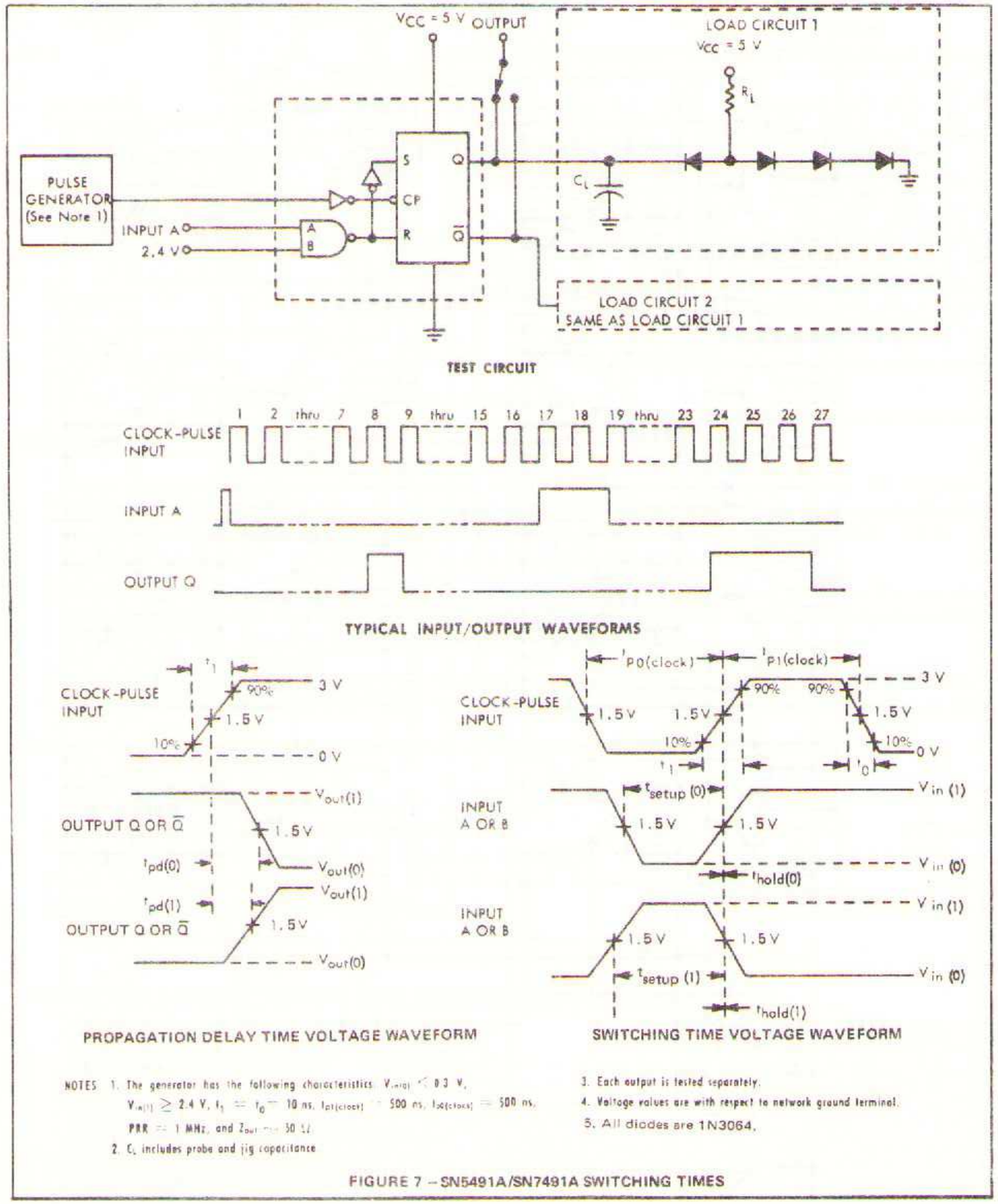


FIGURE 6

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES: 1. The generator has the following characteristics: $V_{out(0)} \leq 0.3$ V, $V_{out(1)} \geq 2.4$ V, $t_1 = t_0 = 10$ ns, $t_{pi(clock)} = 500$ ns, $t_{pi(clock)} = 500$ ns, PRR = 1 MHz, and $Z_{out} = 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. All diodes are 1N3064.

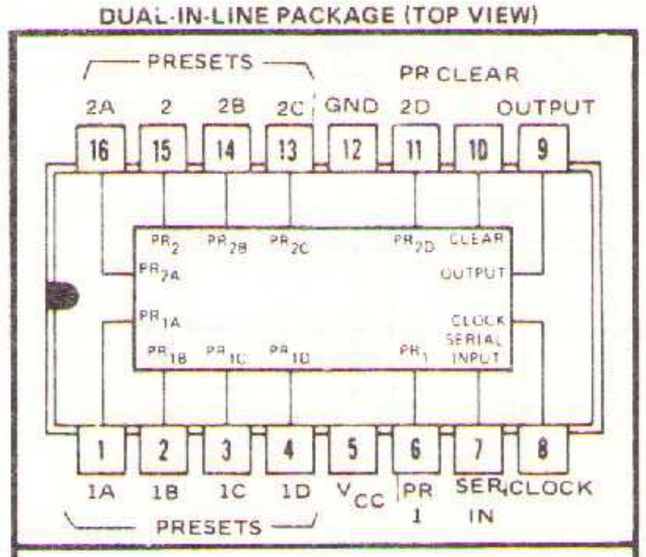
FIGURE 7 – SN5491A/SN7491A SWITCHING TIMES

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS

for application as

- Dual-Source, Parallel-To-Serial Converter
- Serial-In Serial-Out Register

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: High input to clear sets A, B, C and D to logical 0.

description

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input and either preset 1 or preset 2 must be at a logical 0 when clocking occurs.

This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits, noise margins are typically one volt. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 25 nanoseconds.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range: SN5494 Circuits	−55°C to 125°C
SN7494 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. The voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5494 Circuits	4.5	5	5.5	V
SN7494 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time: $t_{setup(1)}$	35			ns
$t_{setup(0)}$	25			ns
Serial Input Hold Time, t_{hold}	0			

NOTE: 1. These voltage values are with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

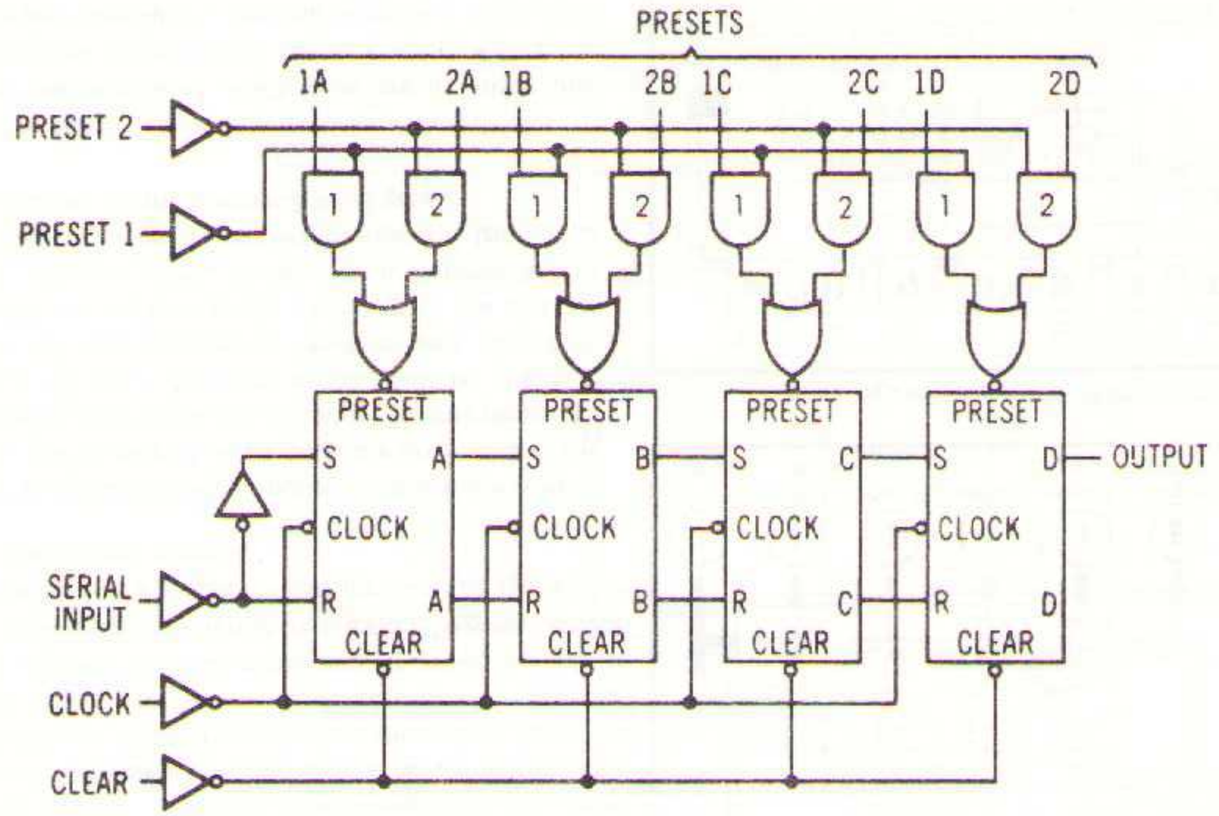
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit input current§	V_{CC} = MAX, V_{out} = 0	SN5494	−20		−57	mA
			SN7494	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	SN5494		35	50	mA
			SN7494		35	58	mA

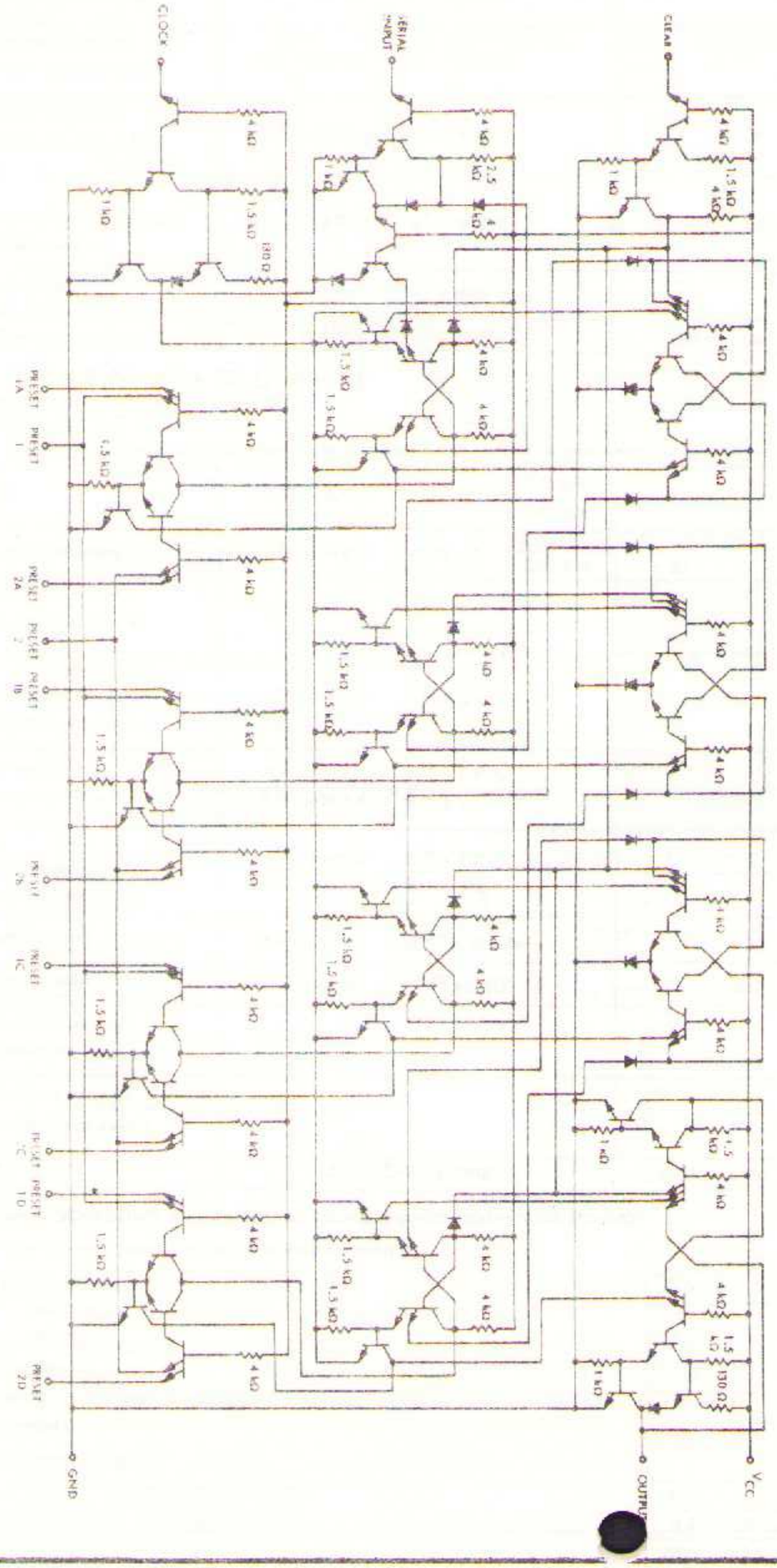
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			40	ns

functional block diagram





Component values shown are nominal.

A TTL MSI PARALLEL-IN PARALLEL-OUT REGISTER

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

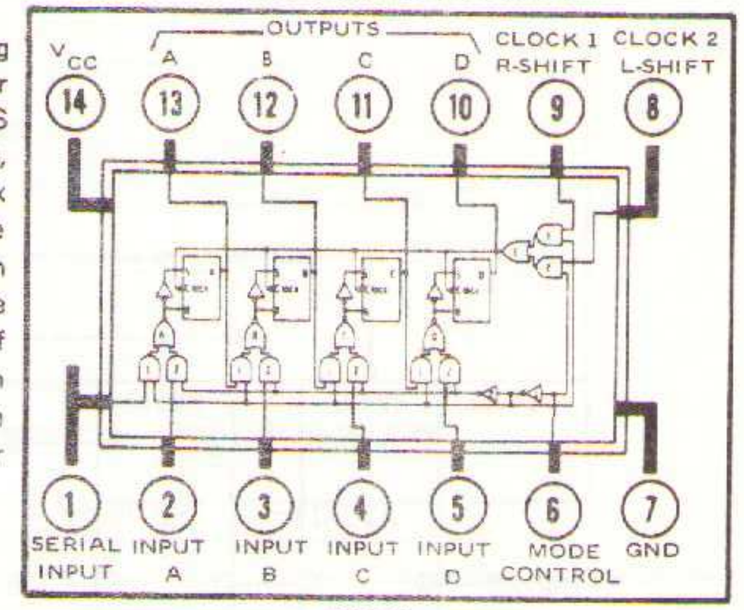
description

This monolithic shift register, utilizing transistor-transistor-logic (TTL) circuits in the familiar Series 54/74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR-INVERT gates, one AND-OR gate, and six inverter-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shifter or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

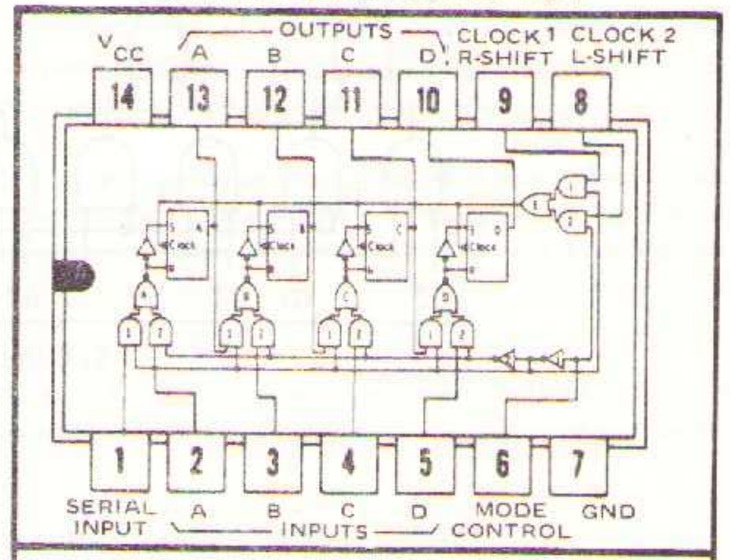
When a logical 0 level is applied to the mode control input, the number-1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number-2 AND gates.

When a logical 1 level is applied to the mode control input, the number-1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number-2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (D_{out} to input C, and etc.), and serial data is entered at input D.

S
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a logical 1 to a logical 0.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is typically 250 milliwatts.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Case Temperature Range: SN5495S Circuits . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5495J, SN5495N Circuits . . . . . −55°C to 125°C
SN7495 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5495 Circuits	4.5	5	5.5	V
SN7495 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output			10	
Width of Clock Pulse $t_{p(clock)}$ (See Figure 9): SN5495 Circuits	20	10		ns
SN7495 Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Figure 9)	20	10		ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Figure 9)	0	−10		ns
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 input)	20			ns
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 input)	20			ns
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 input)	10			ns
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 input)	10			ns

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

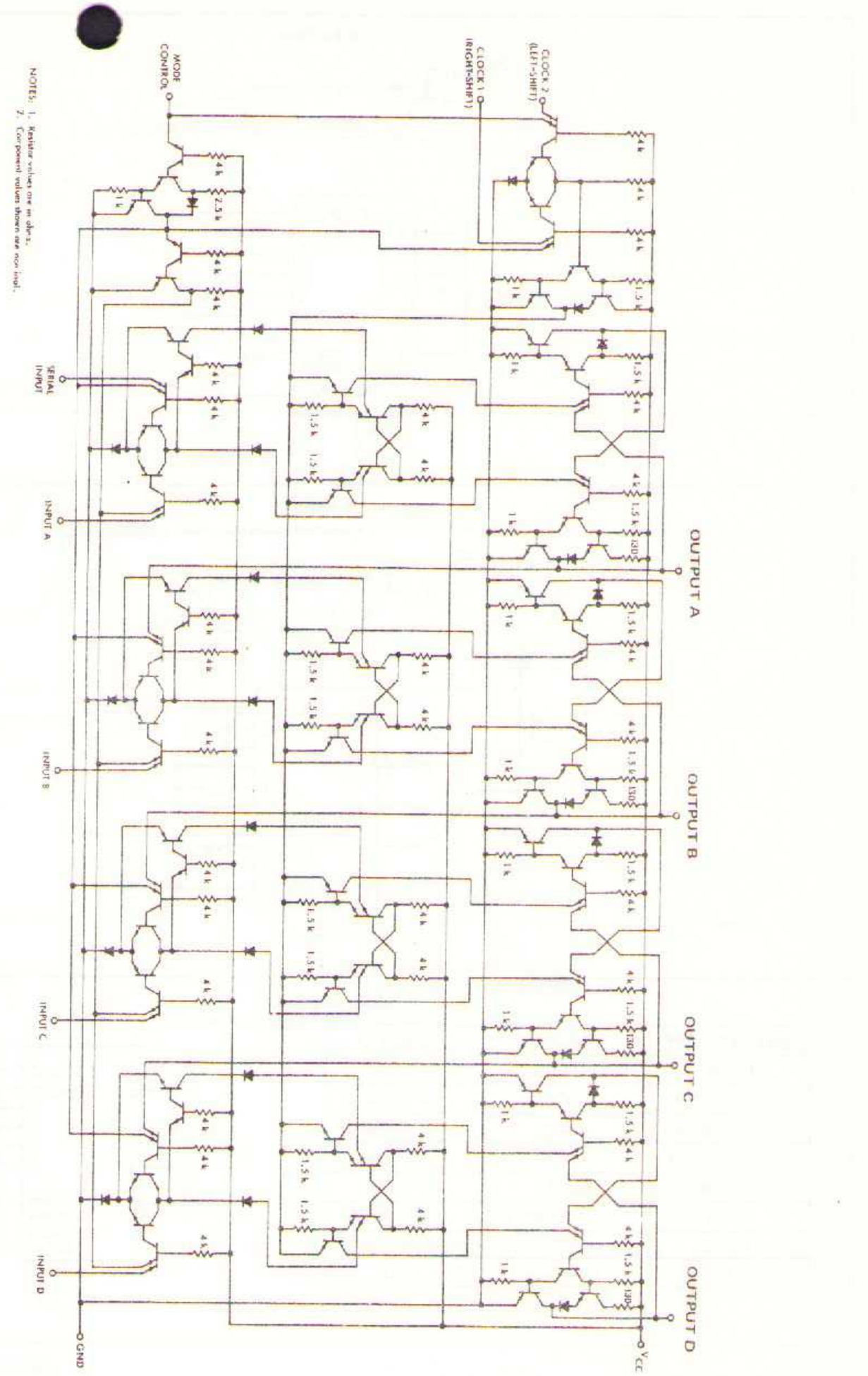
electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN,	I_{load} = −400 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN,	I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX,	V_{in} = 0.4 V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX,	V_{in} = 2.4 V			80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current§	7	V_{CC} = MAX		−18		−57	mA
I_{CC}	Supply current	8	V_{CC} = MAX	SN5495		50	72	mA
				SN7495		50	82	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 15 pF,	R_L = 400 Ω	20	31		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF,	R_L = 400 Ω		26	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF,	R_L = 400 Ω		24	35	ns



d-c test circuits†

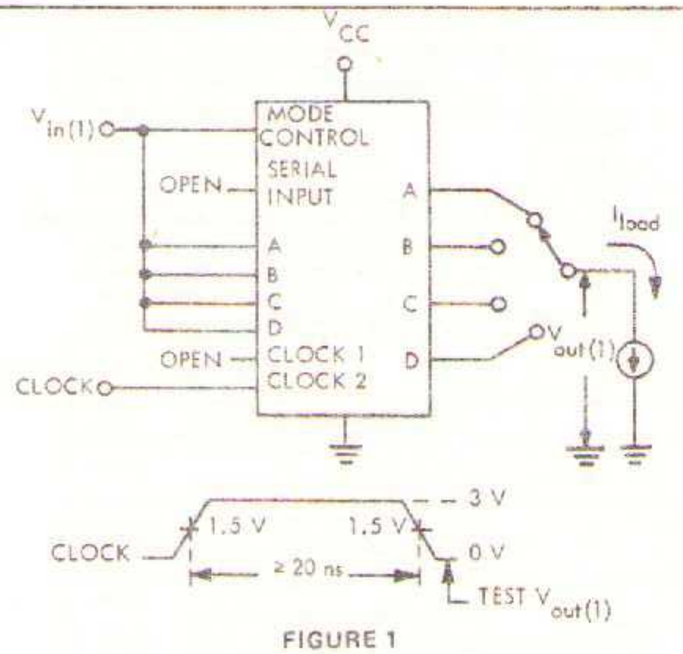


FIGURE 1

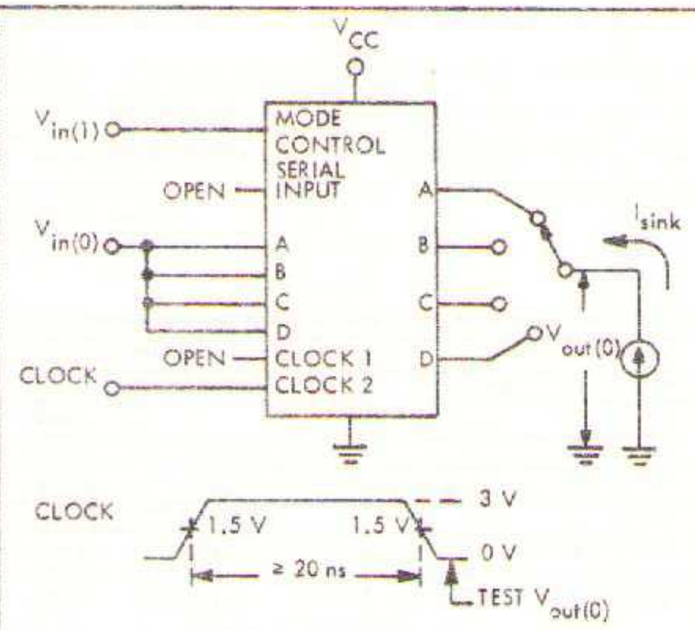


FIGURE 2

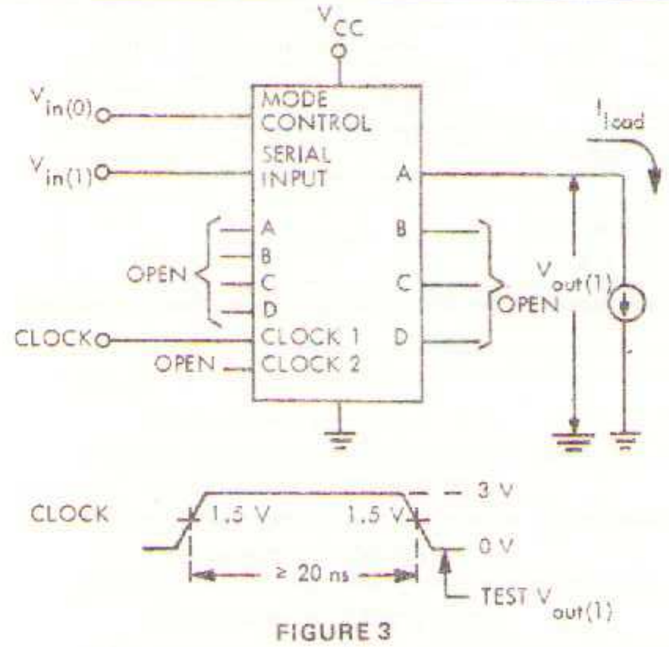


FIGURE 3

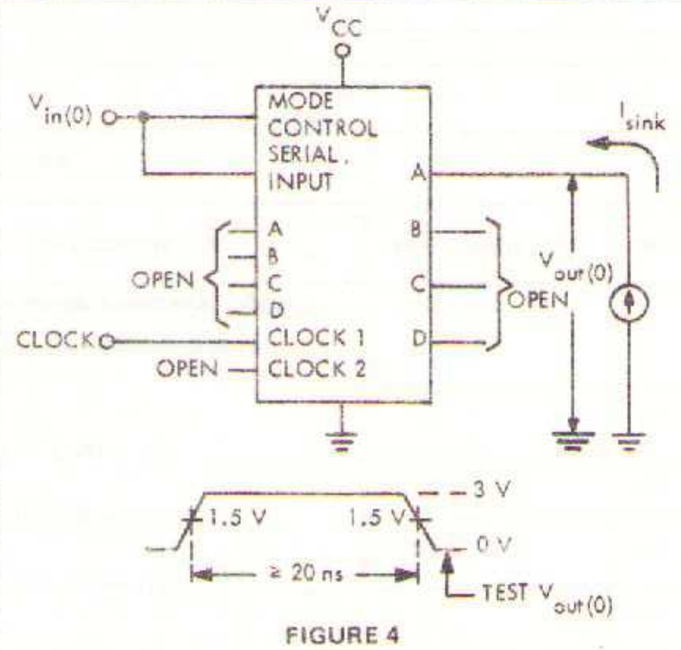
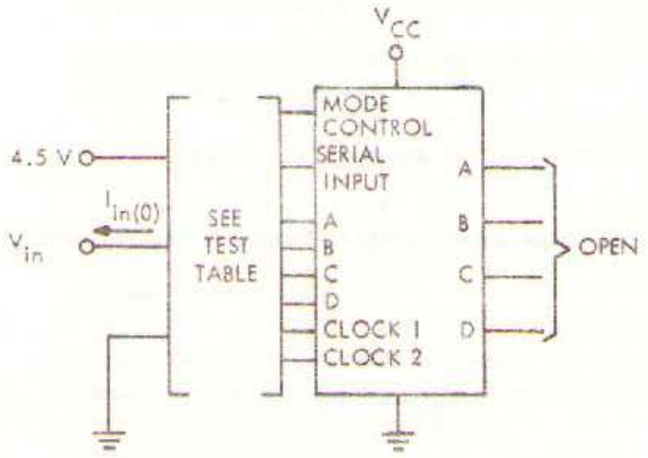


FIGURE 4



1. Each input is tested separately.

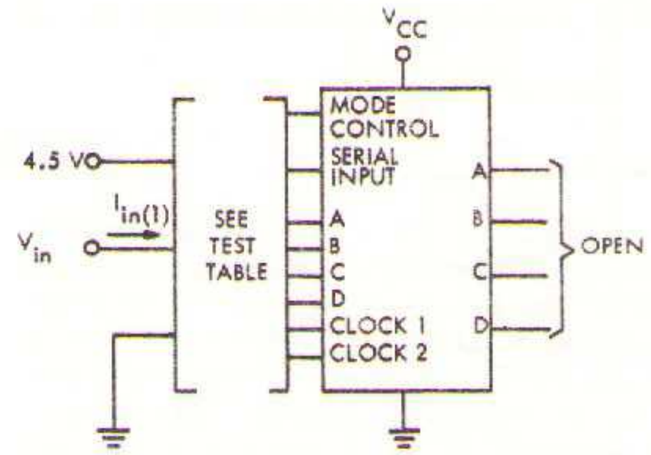
TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
INPUT A	MODE CONTROL	NONE
INPUT B	MODE CONTROL	NONE
INPUT C	MODE CONTROL	NONE
INPUT D	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

FIGURE 5

†Arrows indicate actual direction of current flow.

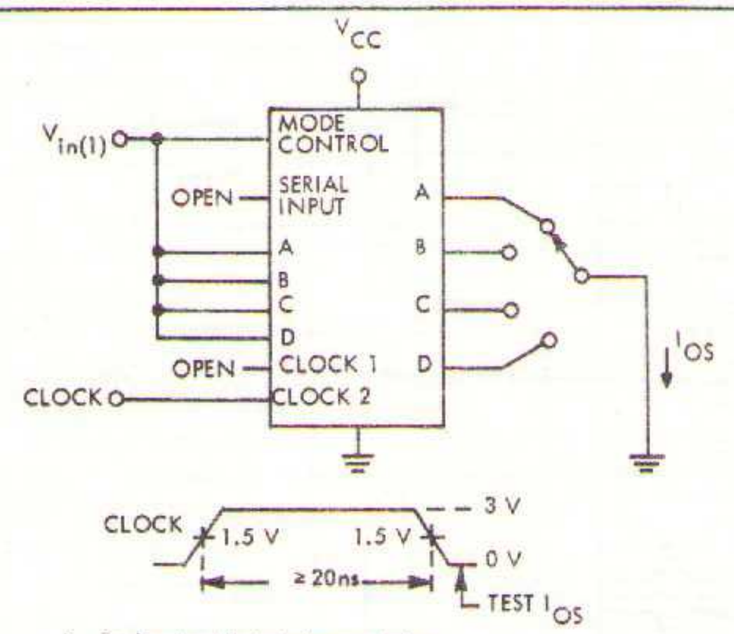
d-c test circuits† (continued)



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
INPUT A	NONE	MODE CONTROL
INPUT B	NONE	MODE CONTROL
INPUT C	NONE	MODE CONTROL
INPUT D	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

FIGURE 6



1. Each output is tested separately.

FIGURE 7

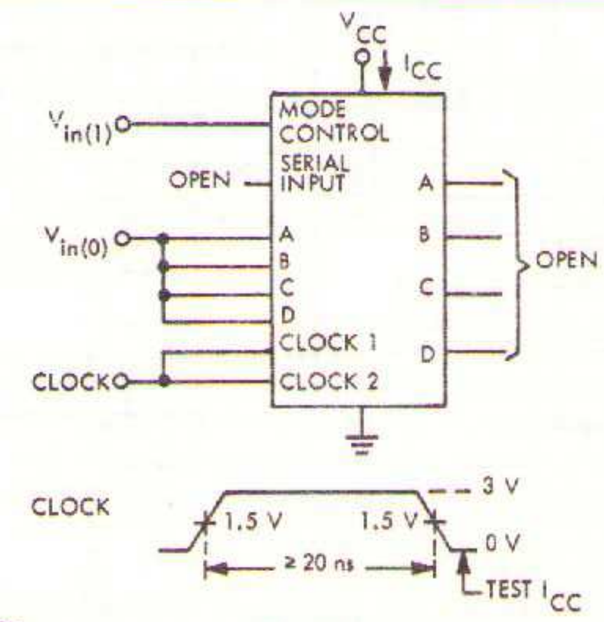
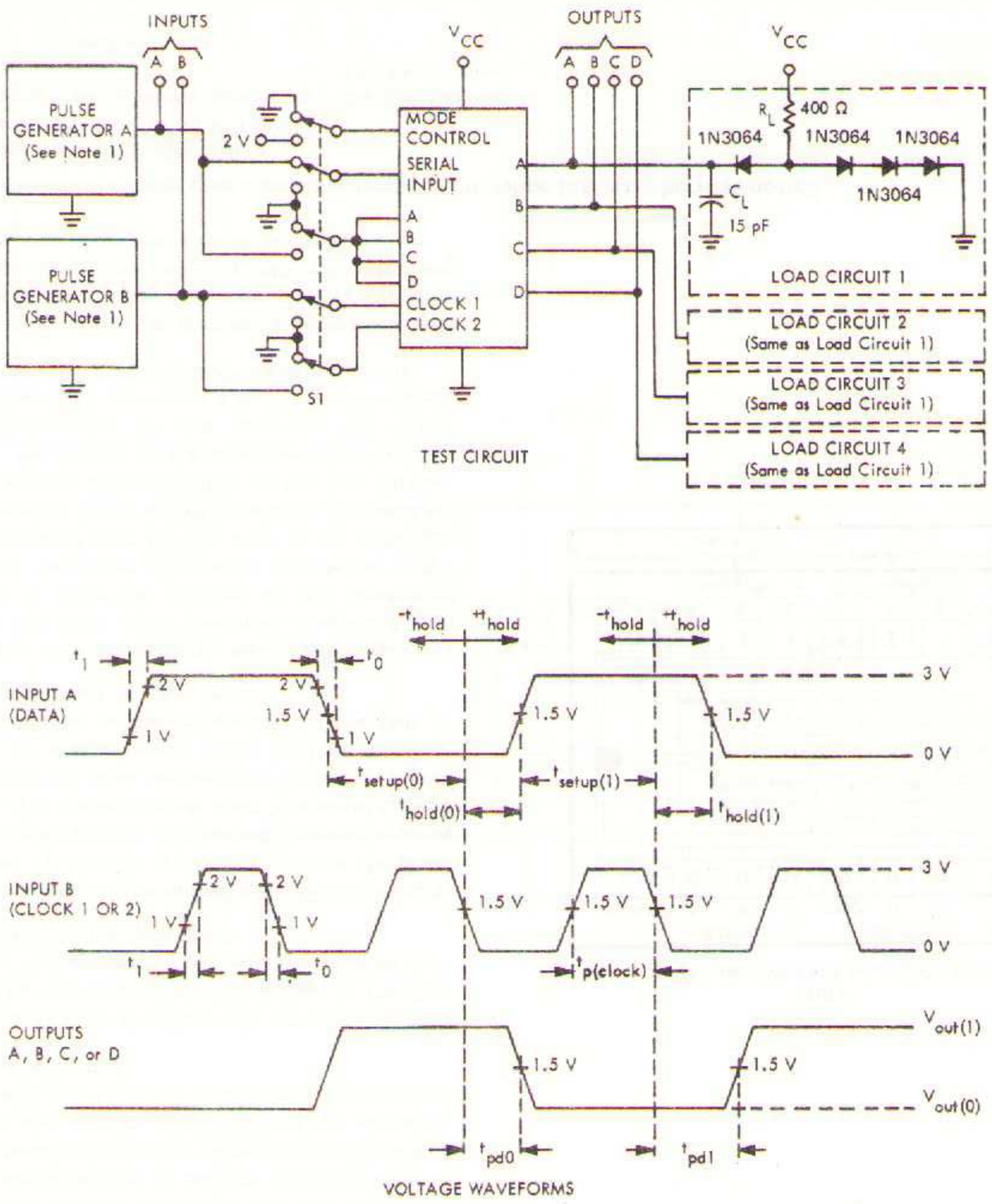


FIGURE 8

†Arrows indicate actual direction of current flow.

switching charateristics

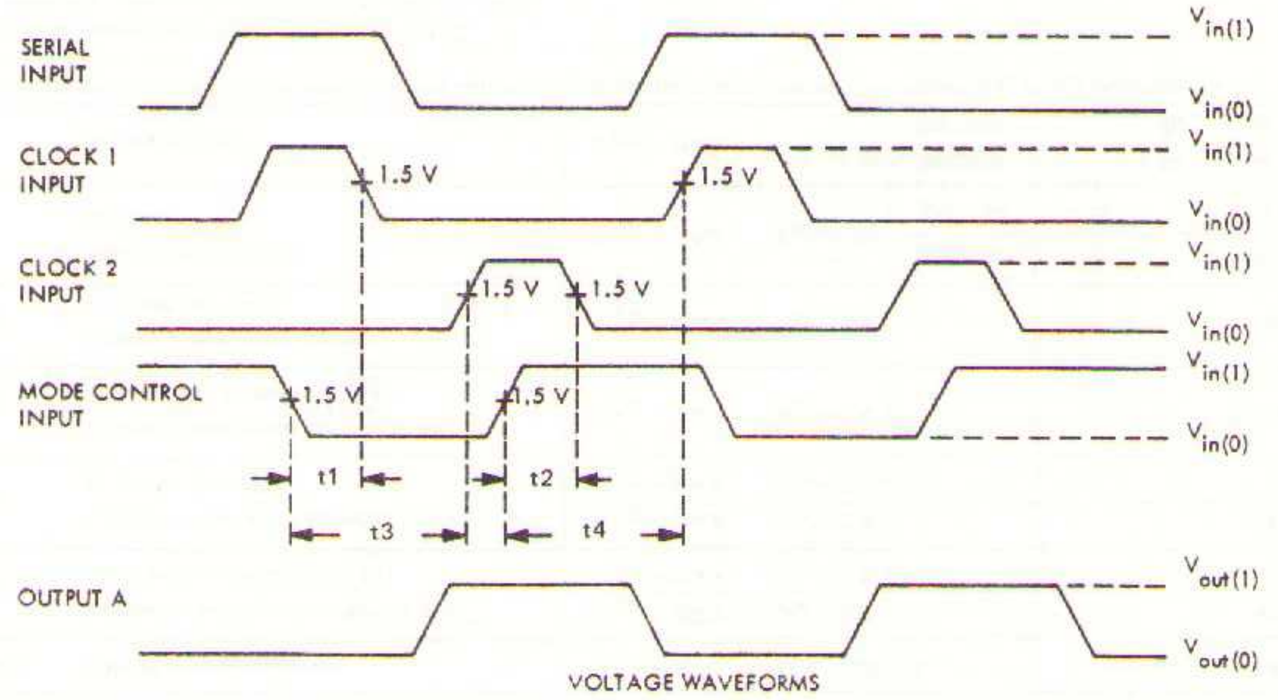


NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A: $t_p \geq 20$ ns and PRR = 500 kHz. For pulse generator B: $t_p \geq 15$ ns and PRR = 1 MHz. When testing f_{max} vary PRR.

2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

recommended mode control setup times



NOTE: Input A is at $V_{in(0)}$.

FIGURE 10–MODE CONTROL SETUP TIMES

TTL MSI MULTIFUNCTION SHIFT REGISTERS

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

description

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

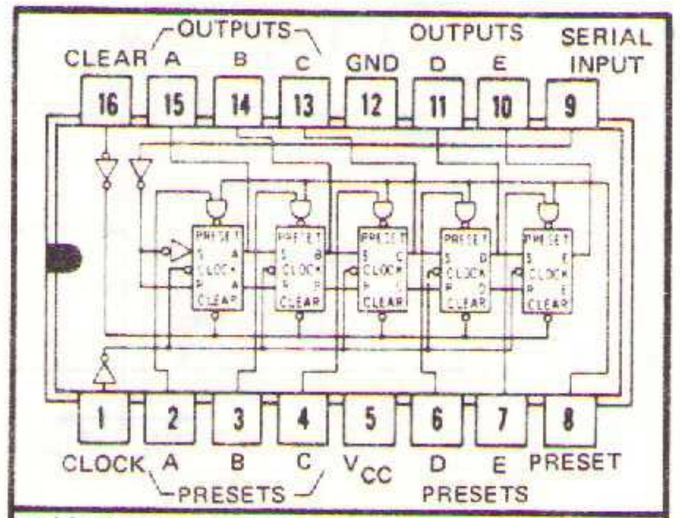
All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Typically, average power dissipation is 240 milliwatts, and propagation delay time is 25 nanoseconds.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input of clear sets all outputs to logical 0.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5496 Circuits . . . . . −55°C to 125°C
SN7496 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

		MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN5496 Circuits	4.5	5	5.5	V
	SN7496 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output				10	
Width of Clock Pulse, $t_{p(clock)}$		35			ns
Width of Clear Pulse, $t_{p(clear)}$		30			ns
Width of Preset Pulse, $t_{p(preset)}$		30			ns
Serial Input Setup Time, t_{setup}		30			ns
Serial Input Hold Time, t_{hold}		0			ns

NOTE 1: This voltage value is with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

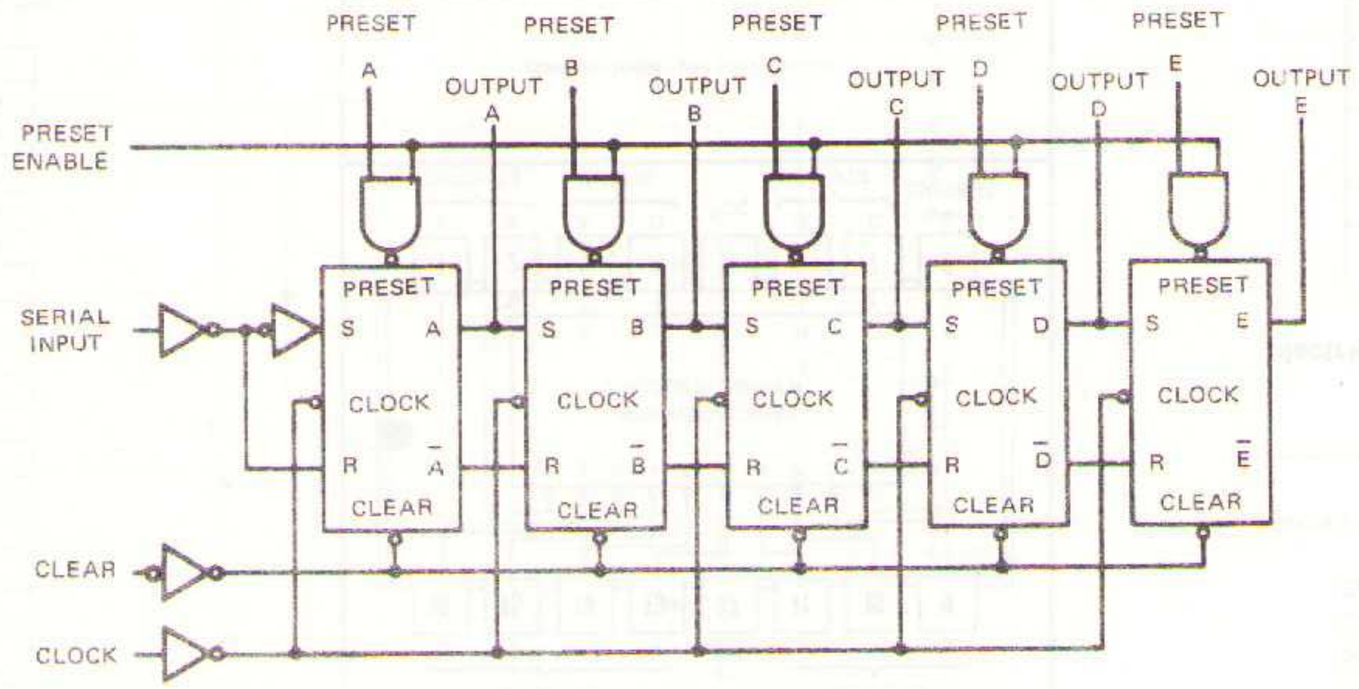
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset (pin 8)	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset (pin 8)	V_{CC} = MAX, V_{in} = 2.4 V				200	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset (pin 8)	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset (pin 8)	V_{CC} = MAX, V_{in} = 0.4 V				−8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_{out} = 0	SN5496	−20		−57	mA
			SN7496	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	SN5496		40	68	mA
			SN7496		48	79	mA

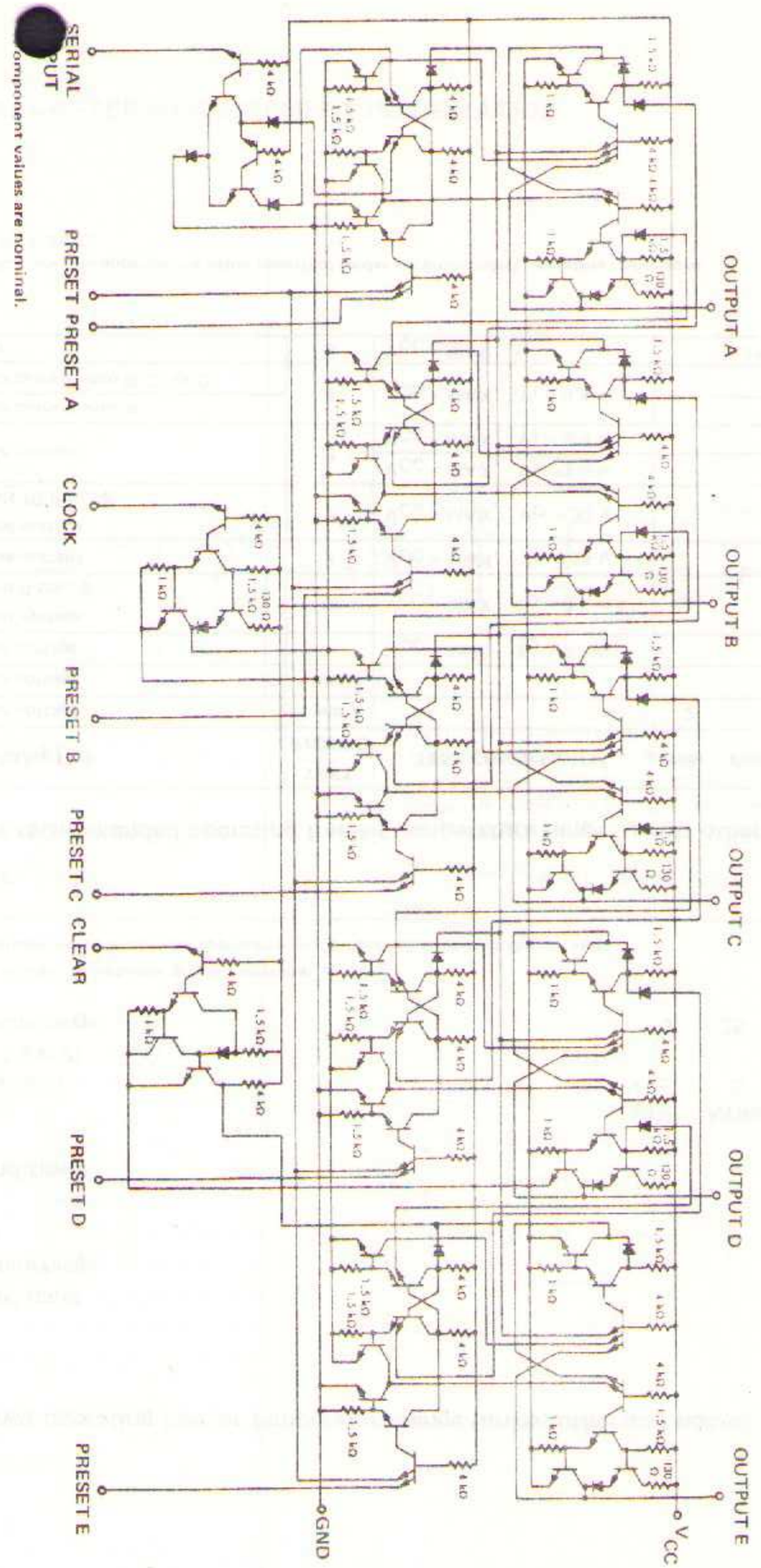
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	C_L = 15 pF, R_L = 400 Ω		28	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			55	ns

functional block diagram





Component values are nominal.

- Drives gas-filled cold-cathode indicator tubes directly
- Fully decoded inputs ensure all outputs are off for invalid codes
- Input clamping diodes minimize transmission-line effects
- Power dissipation typically 55 mW

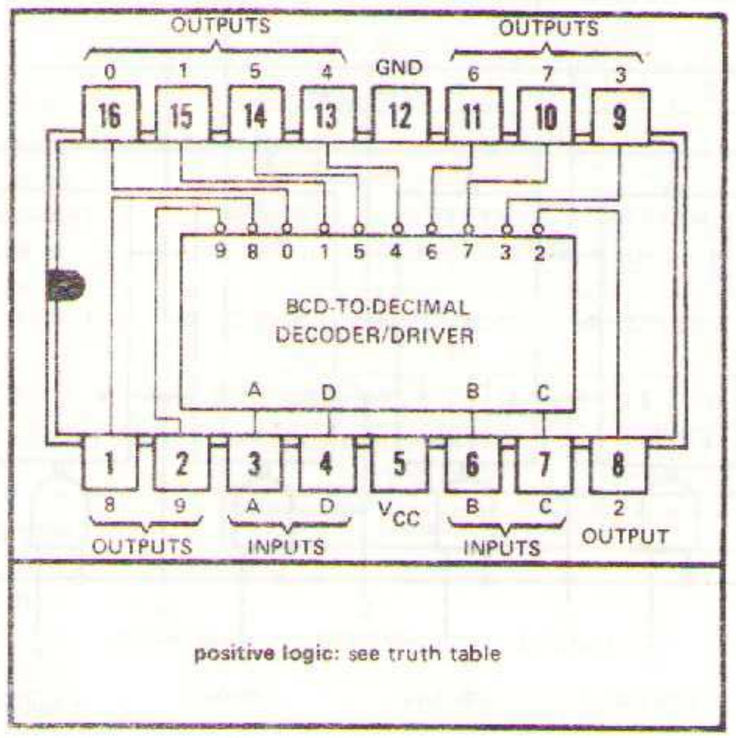
logic

TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level
†All other outputs are off

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

description

The SN74141 is a second-generation BCD-tc-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the SN74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 70 volts.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 milliwatts, which is about one-half the power requirement of earlier designs. The SN74141 is characterized for operation over the temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC}	7 V
Input voltage (see Note 1)	5.5 V
Current into any output (off-state)	2 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC} (see Note 1)	4.75	5	5.25	V
Output voltage (see Notes 1 and 2)			65	V
Operating free-air temperature range	0	25	70	°C

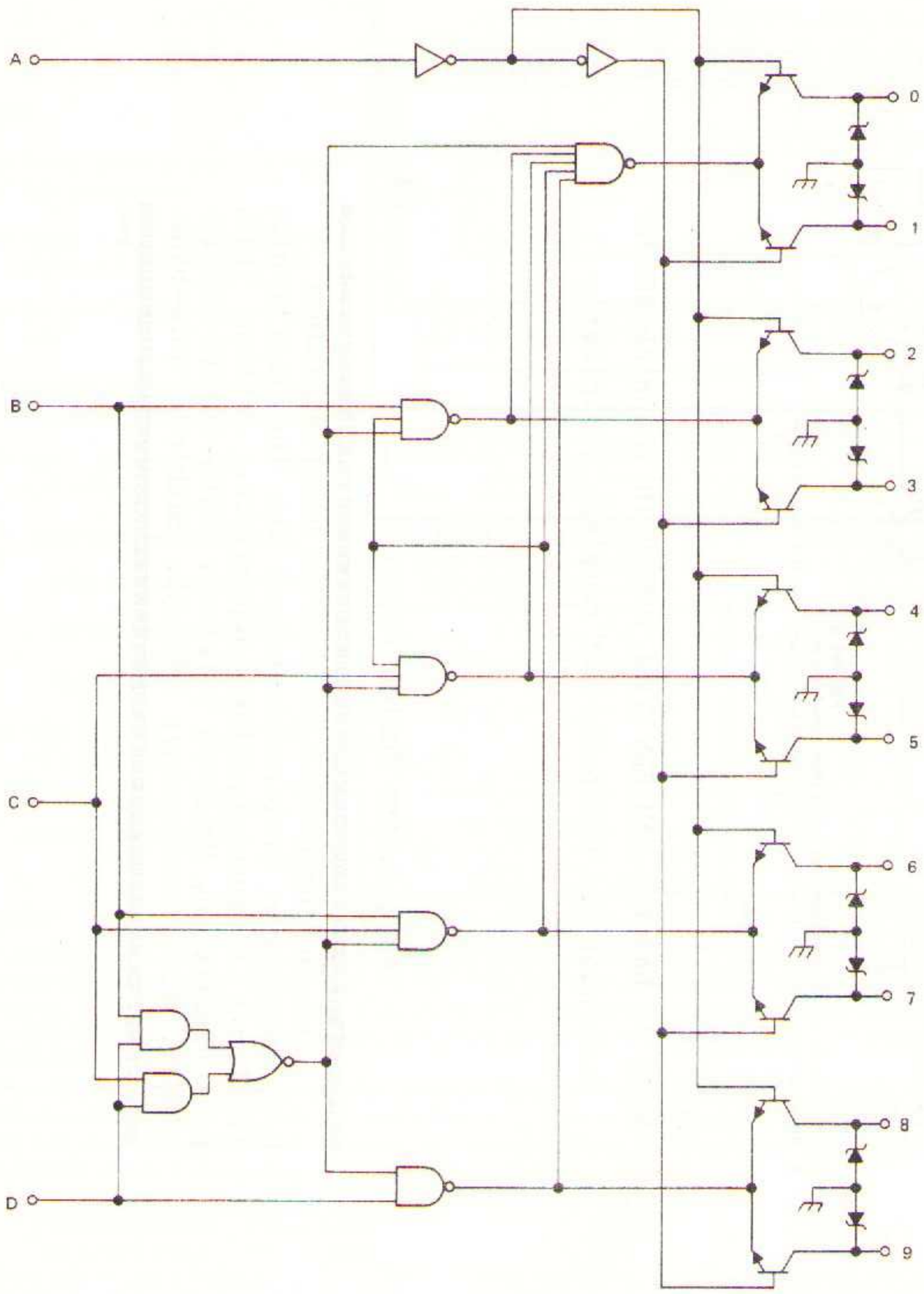
NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2		2			V
V_{IL}	Low-level input voltage	1 and 2				0.8	V
$V_{O(on)}$	On-state output voltage	1	V_{CC} = MIN, I_O = 7 mA			2.5	V
$V_{O(off)}$	Off-state output voltage for input counts 0 thru 9	2	V_{CC} = MAX, I_O = 0.5 mA	65			V
$I_{O(off)}$	Off-state reverse current	2	V_{CC} = MAX, V_O = 55 V			50	μA
$I_{O(off)}$	Off-state reverse current for input counts 10 thru 15	2	V_{CC} = MAX, V_O = 30 V			5	μA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current into A	4	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{IL}	Low-level input current into B, C, or D					−3.2	mA
I_{CC}	Supply current	3	V_{CC} = MAX		11	16	mA

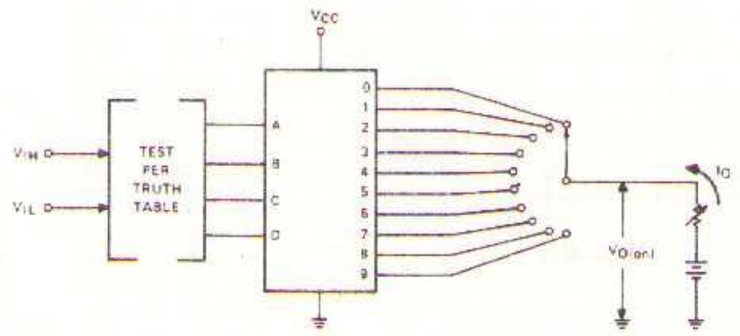
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡This typical value is at V_{CC} = 5 V, T_A = 25°C.

functional block diagram



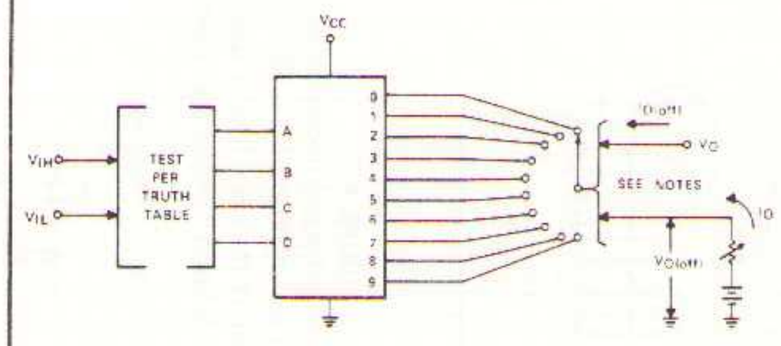
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



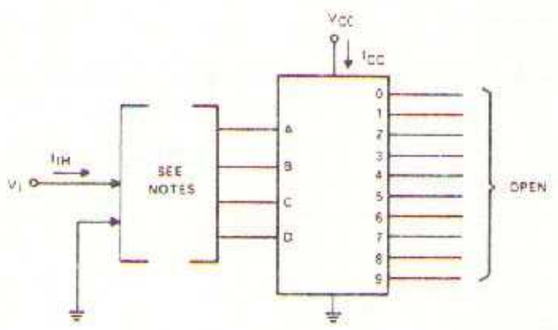
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, $V_{O(on)}$



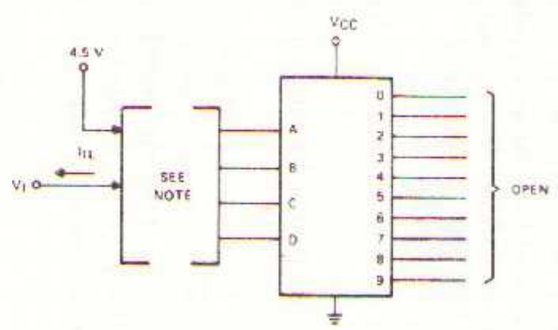
A. Each output is tested separately.
B. $V_{O(off)}$ is tested at I_O = 0.5 mA and $I_{O(off)}$ is tested at V_O = 55 V for all input counts. $I_{O(off)}$ is tested also at V_O = 30 V for input counts 10 through 15.

FIGURE 2–V_{IH}, V_{IL}, $I_{O(off)}$, $V_{O(off)}$



A. When testing I_{IH}, each input is tested separately with all other inputs grounded.
B. When testing I_{CC}, all inputs are grounded.

FIGURE 3–I_{IH}, I_{CC}



Each input is tested separately, with all other inputs at 4.5 V.

FIGURE 4–I_{IL}

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TYPICAL APPLICATION DATA

general

When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.

driving indicator tubes

As shown in figure A, the SN74141 requires no external components for driving cold-cathode indicator tubes. The versatility here is limited only by the system capability to control the data inputs.

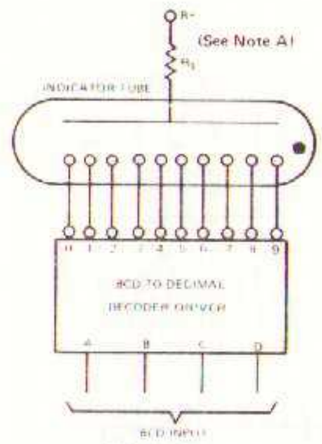


FIGURE A

A suggested method for blanking extraneous zeros is shown in figure B. Any input count above decimal 9 may be used for blanking. In the following application decimal 12 is used. When the most-significant bit (MSB) or the least-significant bit (LSB) is decimal 0(0000), that indicator is blanked while decimal 12 (binary 1100) is applied to the SN74141 inputs causing all the outputs to be off. If the MSB or LSB is decimal 0 and being blanked, this signal is gated with and blanks the next smaller digit. This scheme is easily expandable to n-digits.

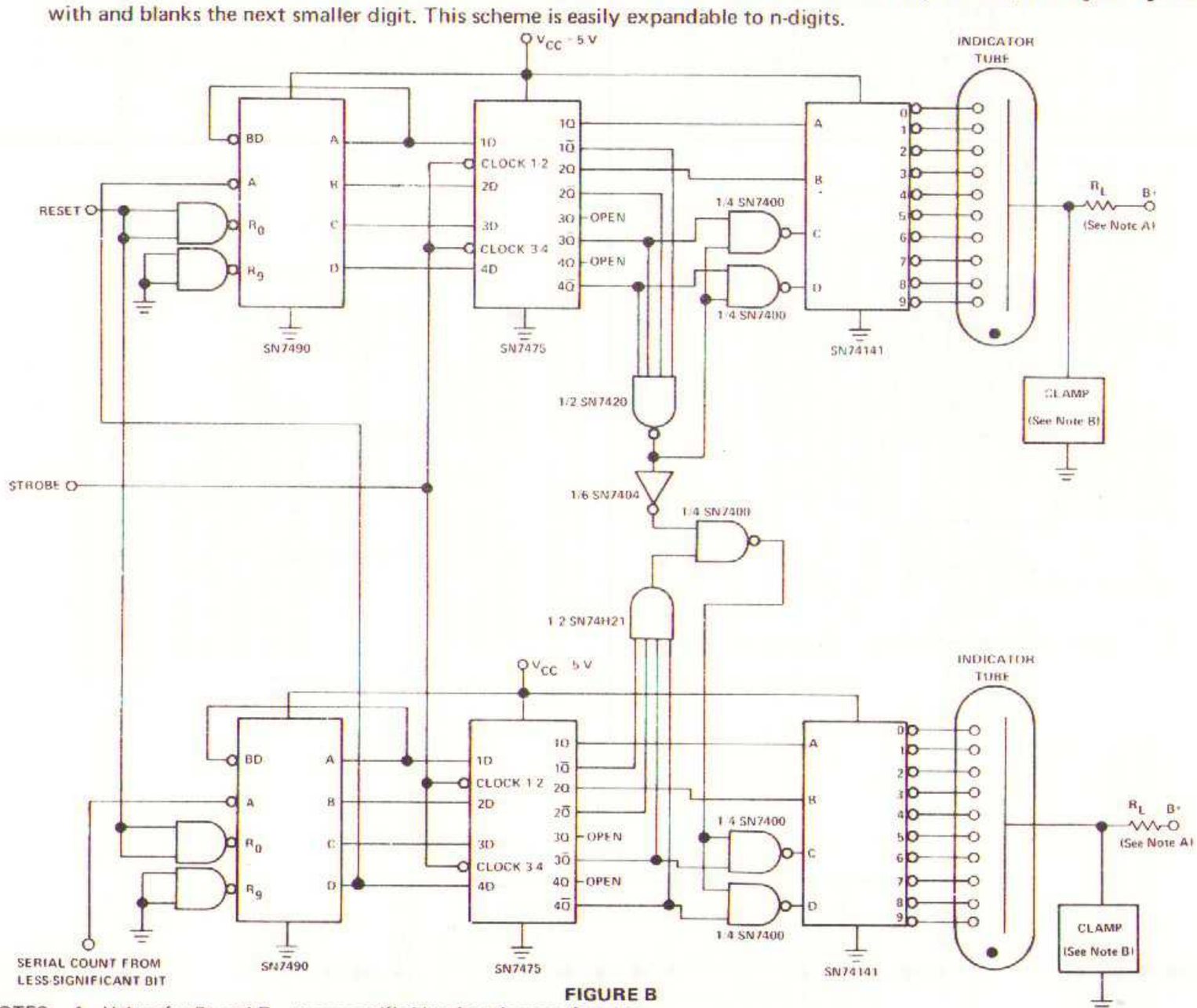


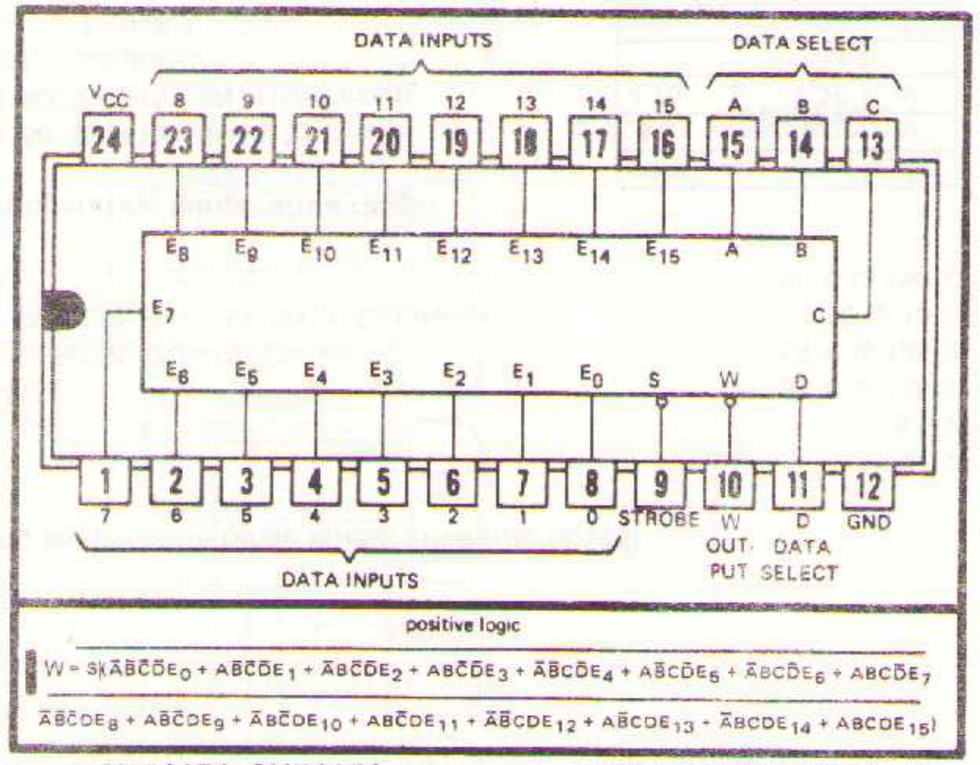
FIGURE B

NOTES: A. Values for B+ and R_L are as specified by the tube manufacturer.
B. Blanking is assured only if the anode of the indicator tube is clamped at 150 volts maximum.

features

- selects one-of-sixteen (or one-of-eight) data sources
- serves as a five-variable-function generator (SN54150, SN74150)
- performs parallel-to-serial conversion
- permits multiplexing from N-lines to 1-line
- input-clamping diodes simplify system design
- typical propagation delay times:
  - through 4 select levels – 28 ns
  - through 3 select levels – 20 ns
  - data input to output – 10 ns
- high fan-out, low impedance, totem-pole outputs
- fully compatible with TTL, DTL and other MSI circuits

SN54150, SN74150
N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$$W = S(\bar{A}\bar{B}\bar{C}\bar{D}_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7)$$

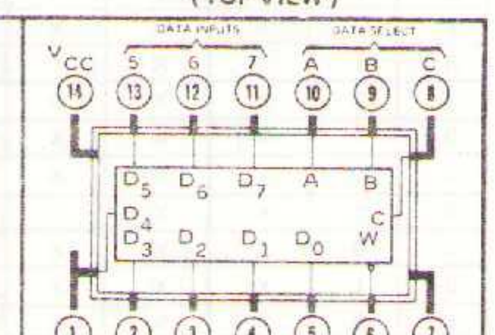
$$\bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

SN54151, SN74151
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

positive logic

$$Y = \bar{S}(\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + \bar{A}B\bar{C}D_2 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7) \quad W = \bar{Y}$$

SN54152, SN74152
S FLAT PACKAGE
(TOP VIEW)



positive logic

$$W = (\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7)$$

description

Each of these monolithic, data selectors/multiplexers contain inverter/drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gate. The SN54151/74151 features complementary outputs whereas the SN54150/SN74150 and SN54152/SN74152 have inverted outputs only. The SN54150/SN74150 and SN54151/SN74151 circuits are provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

These data selectors/multiplexers are fully compatible for use with other TTL or DTL circuits. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

SN54150/SN74150 – 200 milliwatts
SN54151/SN74151 – 145 milliwatts
SN54152/SN74152 – 130 milliwatts

These data selectors feature Series 54H/74H circuitry for the OR function. This is done to minimize the capacitive effects of paralleling the phase-splitter transistors and thus reduce the propagation delay time. The SN54150, SN54151, and SN54152 are characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74150, SN74151 and SN74152 are characterized for operation from 0°C to 70°C.

logic

TRUTH TABLE (SN54150/SN74150 ONLY)

INPUTS																		OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

When used to indicate an input condition, X = LOGICAL 1 OR LOGICAL 0

logic (continued)

TRUTH TABLE (SN54151/SN74151 AND SN54152/SN74152 ONLY)

INPUTS												OUTPUTS	
C	B	A	STROBE(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

NOTES: 1. SN54151/SN74151 only.
2. When used to indicate an input, X = irrelevant.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Case Temperature Range: SN54152 . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN54150, SN54151 Circuits . . . . . −55°C to 125°C
SN74150, SN74151, SN74152 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54150, SN54151, SN54152 Circuits	4.5	5	5.5	V
SN74150, SN74151, SN74152 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N): Logical 0			10	
Logical 1			20	

electrical characteristics (over operating temperature range unless otherwise noted)

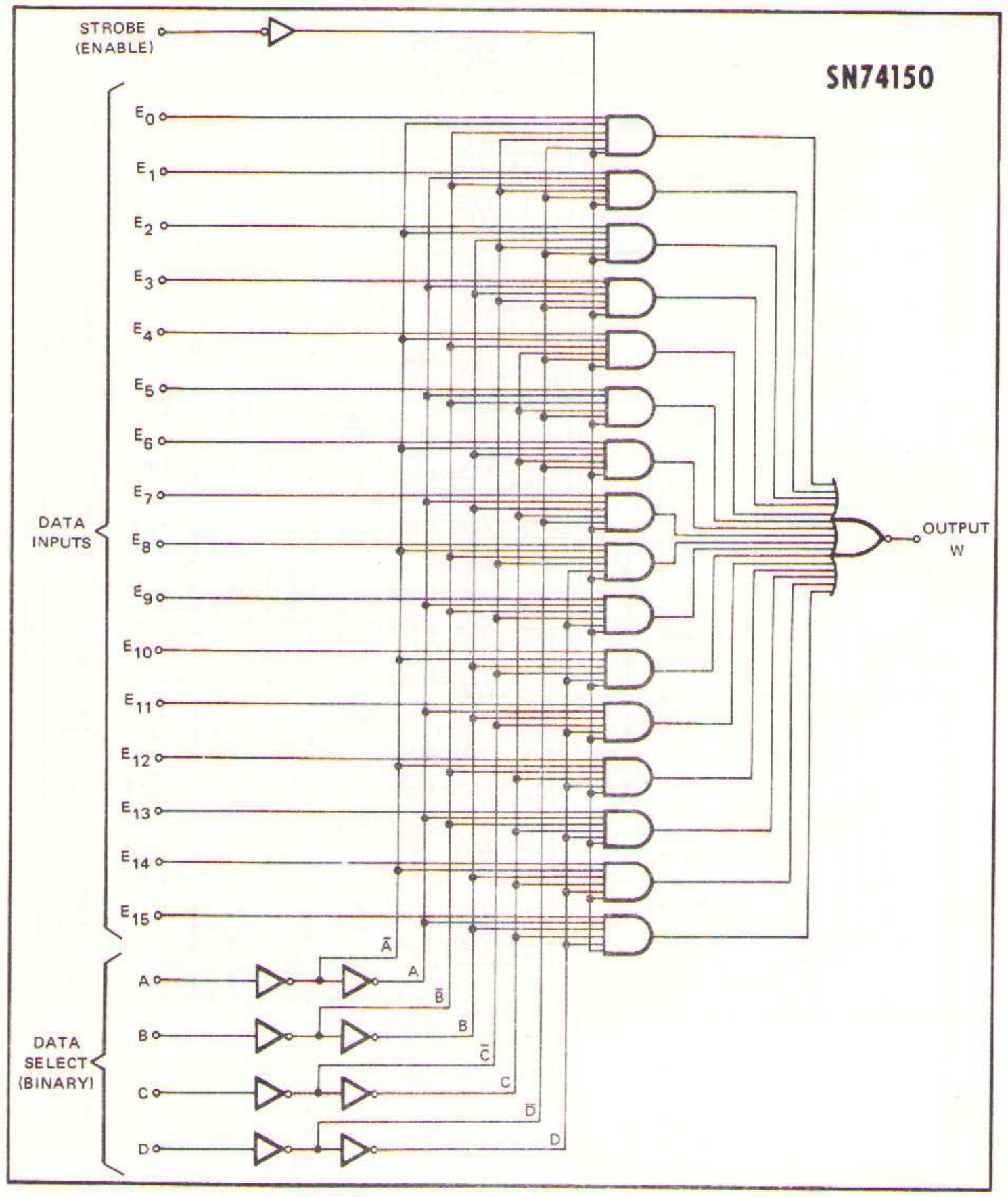
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 AND 2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 AND 2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short circuit output current §	4	V_{CC} = MAX, V_{out} = 0	SN54150, SN54151, SN54152	−20		−55	mA
				SN74150, SN74151, SN74152	−18		−55	mA
I_{CC}	Supply current (SN54150/SN74150)	5	V_{CC} = MAX, V_{in} = 4.5 V			40	68	mA
I_{CC}	Supply current (SN54151/SN74151)	5	V_{CC} = MAX, V_{in} = 4.5 V			29	48	mA
I_{CC}	Supply current (SN54152/SN74152)	5	V_{CC} = MAX, V_{in} = 4.5 V			26	43	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

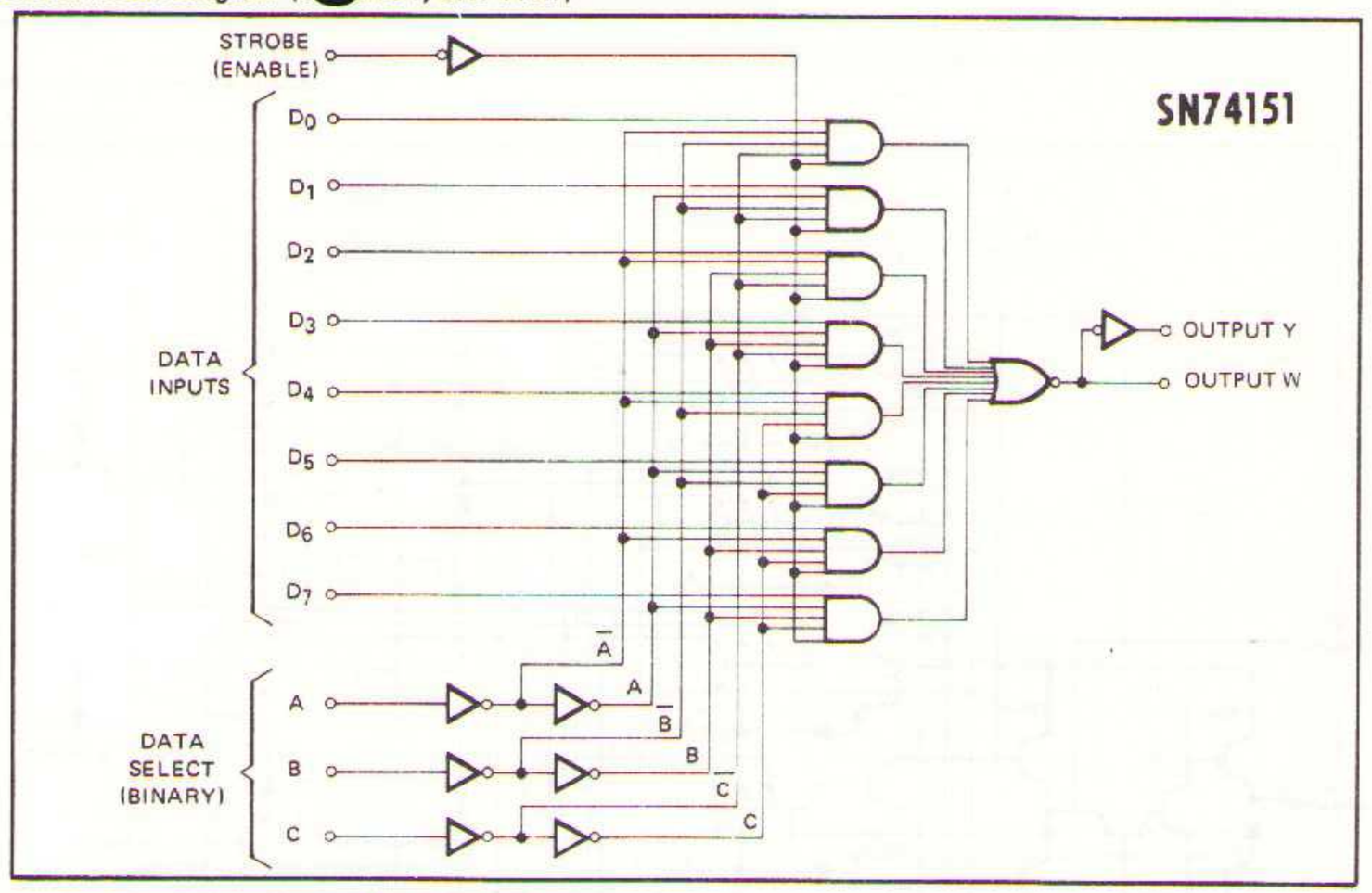
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A, B, or C (4 levels)	Y	6	C_L = 15 pF, R_L = 400 Ω		20	30	ns
t_{pd1}	A, B, or C (4 levels)	Y				35	52	ns
t_{pd0}	A, B, C, or D (3 levels)	W				19	30	ns
t_{pd1}	A, B, C, or D (3 levels)	W				20	30	ns
t_{pd0}	STROBE	Y				19	30	ns
t_{pd1}	STROBE	Y				35	52	ns
t_{pd0}	STROBE	W				21	30	ns
t_{pd1}	STROBE	W				12	20	ns
t_{pd0}	D_0 thru D_7	Y				8.5	14	ns
t_{pd1}	D_0 thru D_7	Y				13	20	ns
t_{pd0}	E_0 thru E_{15}	W				8.5	14	ns
t_{pd1}	E_0 thru E_{15}	W				11	20	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output of [illegible]/SN54151/SN74151 should be shorted at a time.

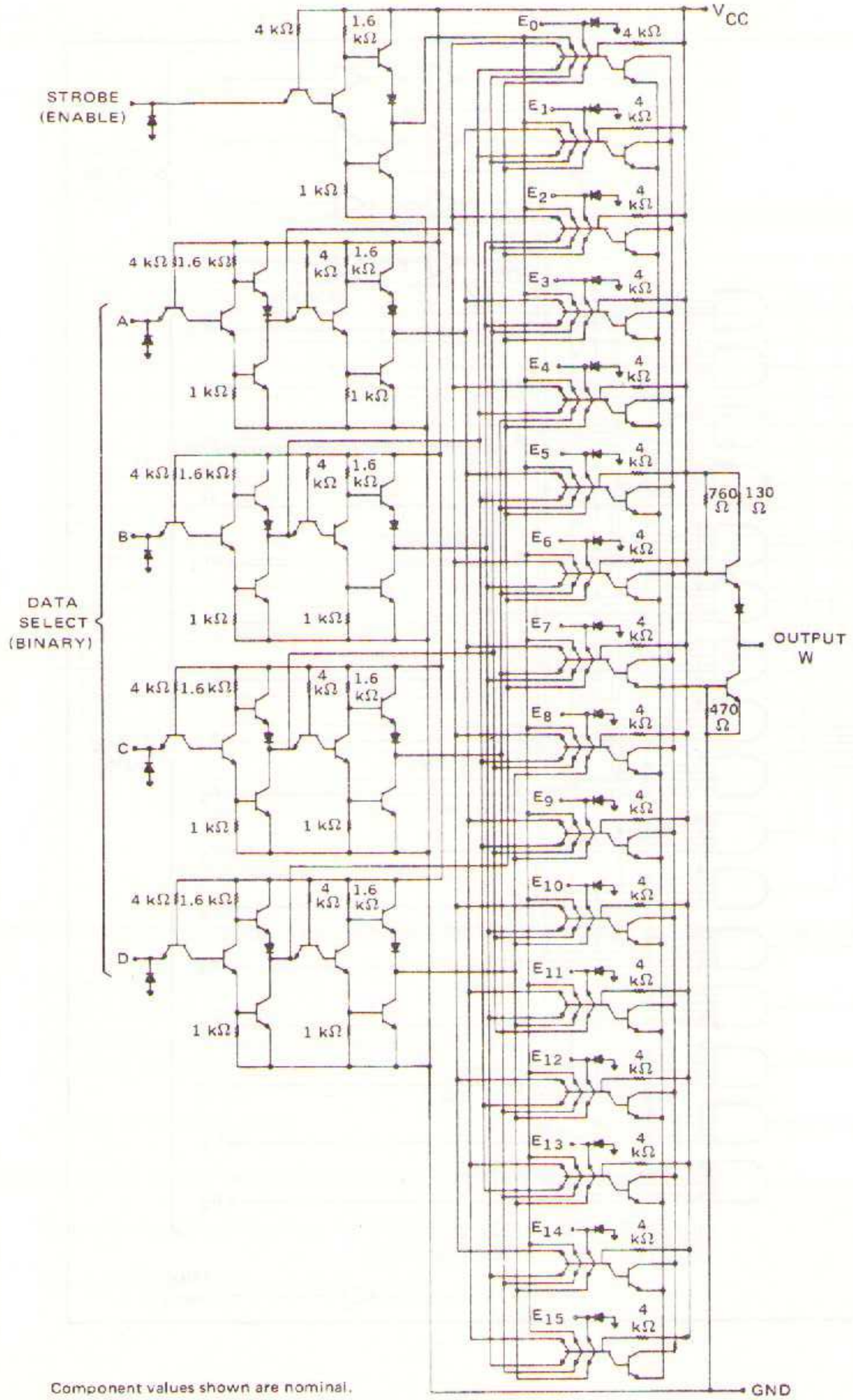
functional block diagram



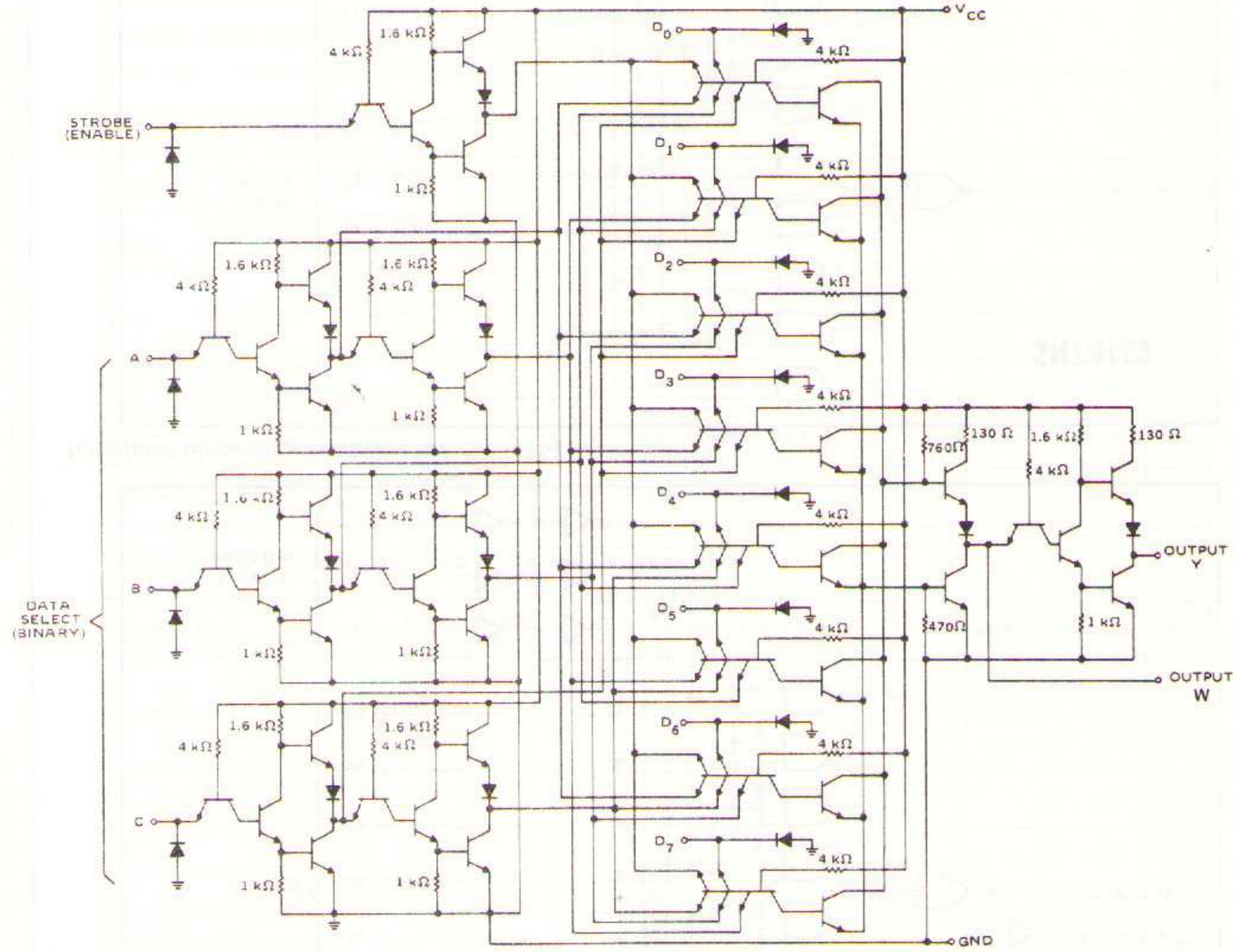
functional block diagram (SN54151, SN74151)



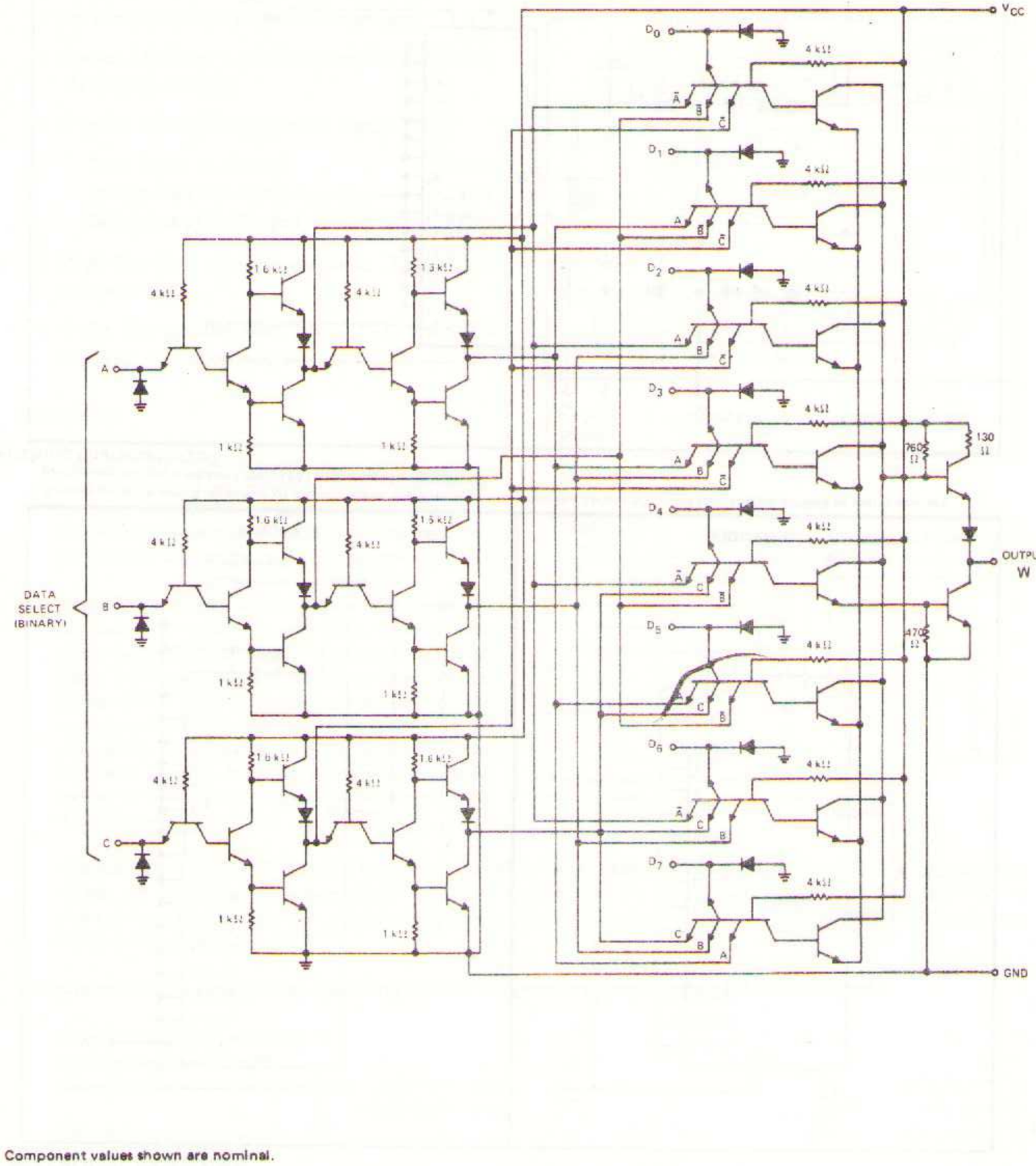
functional block diagram (SN54152, SN74152)



Component values shown are nominal.



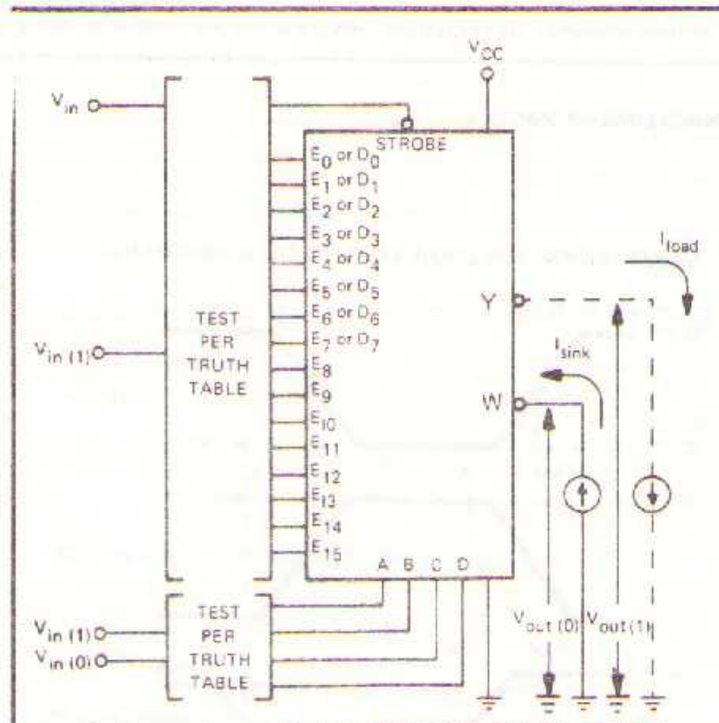
Component values shown are nominal.



Component values shown are nominal.

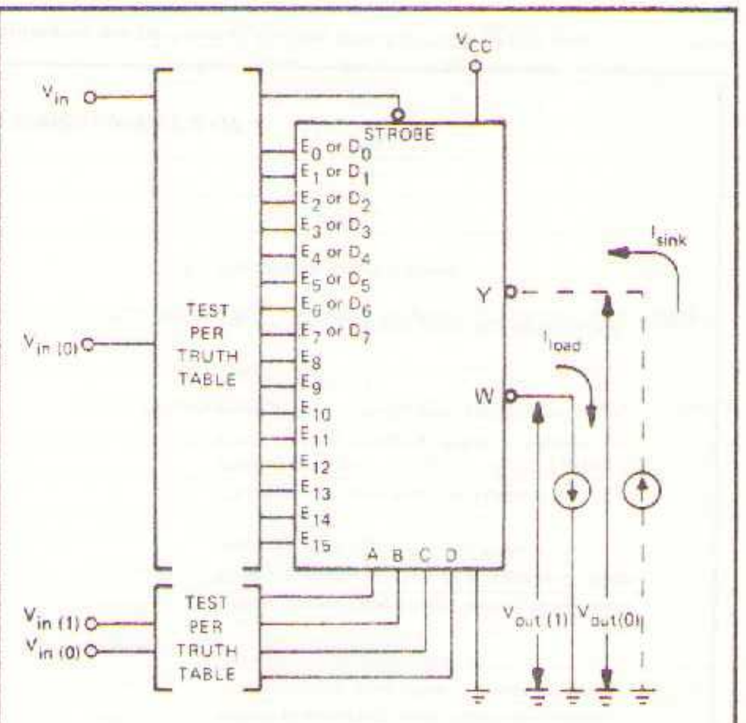
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 code is applied to A, B, C, D; and input/output condition is tested for each step of the code.
2. $V_{in(1)}$ is applied to STROBE at which time $V_{out(0)}$ is measured at Y and $V_{out(1)}$ is measured at W.

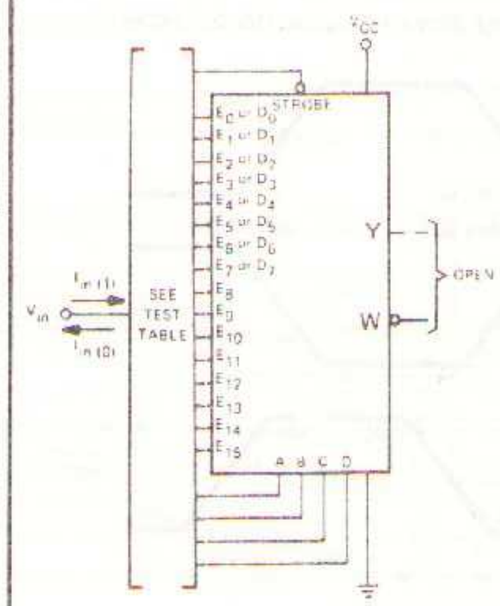
FIGURE 1



1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 is applied to A, B, C, D; and input/output condition is tested for each step of the code.

FIGURE 2

TEST TABLE



INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	0	0	E_0 or D_0	E_{15} or D_7
1	0	0	0	E_1 or D_1	E_{14} or D_6
0	1	0	0	E_2 or D_2	E_{13} or D_5
1	1	0	0	E_3 or D_3	E_{12} or D_4
0	0	1	0	E_4 or D_4	E_{11} or D_3
1	0	1	0	E_5 or D_5	E_{10} or D_2
0	1	1	0	E_6 or D_6	E_9 or D_1
1	1	1	0	E_7 or D_7	E_8 or D_0
0	0	0	1	E_8	E_7
1	0	0	1	E_9	E_6
0	1	0	1	E_{10}	E_5
1	1	0	1	E_{11}	E_4

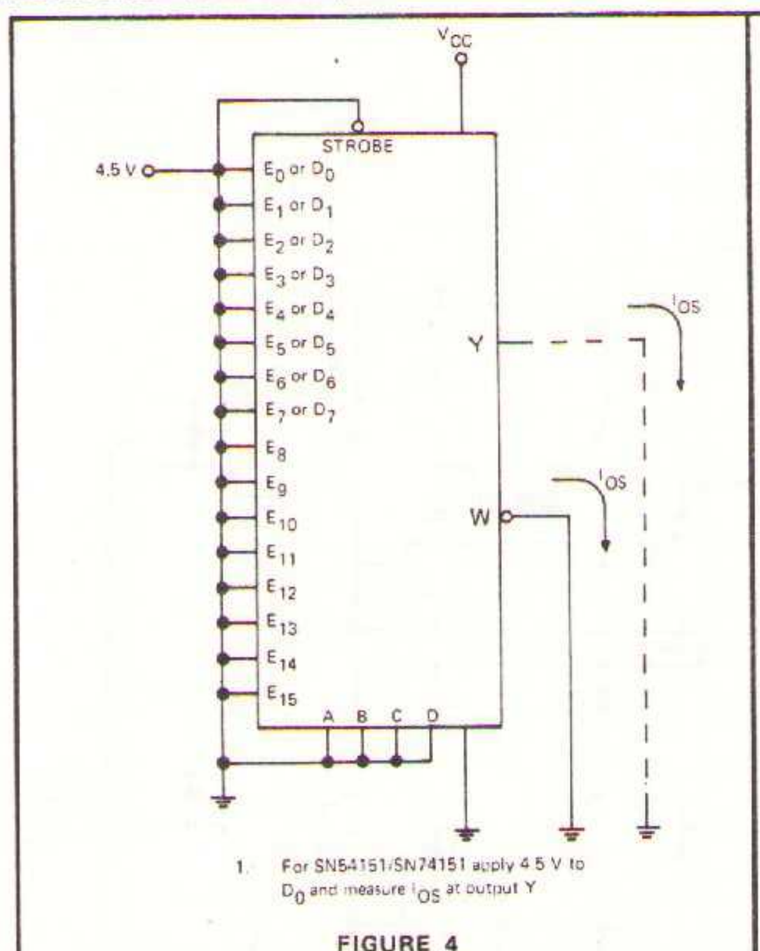
INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	1	1	E_{12}	E_3
1	0	1	1	E_{13}	E_2
0	1	1	1	E_{14}	E_1
1	1	1	1	E_{15}	E_0
0				A	
	0			B	
		0		C	
			0	D	
1					A
	1				B
		1			C
			1		D

FIGURE 3

† Arrows indicate actual direction of current flow. Tests as shown, are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. For SN54151/SN74151 apply 4.5 V to D_0 and measure I_{OS} at output Y

FIGURE 4

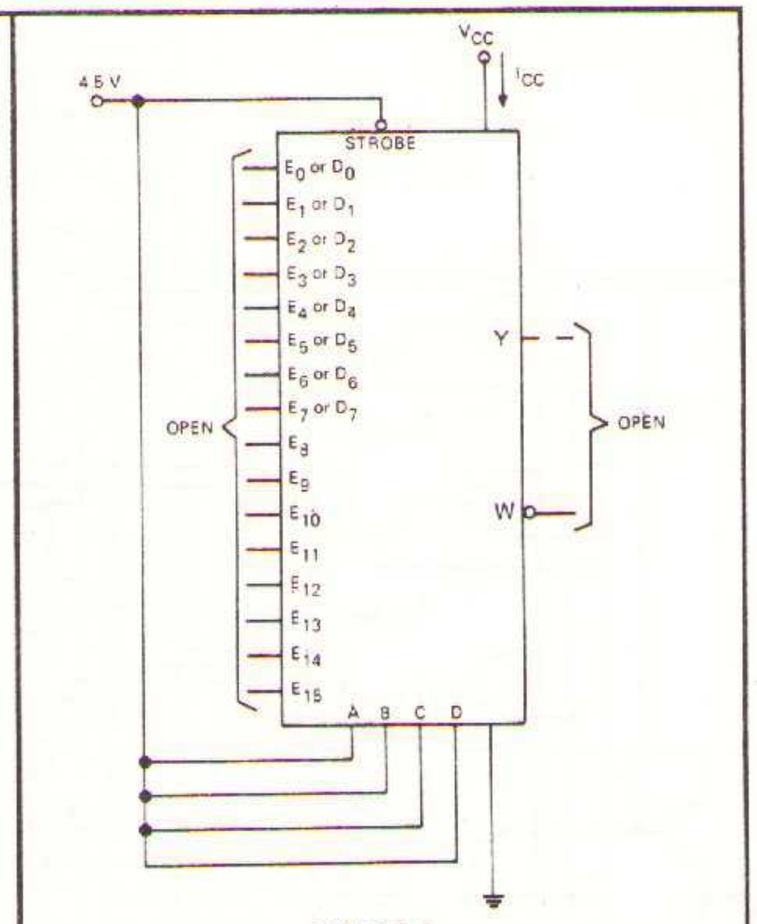


FIGURE 5

† Arrows indicate actual direction of current flow. Tests, as shown are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

switching characteristics†

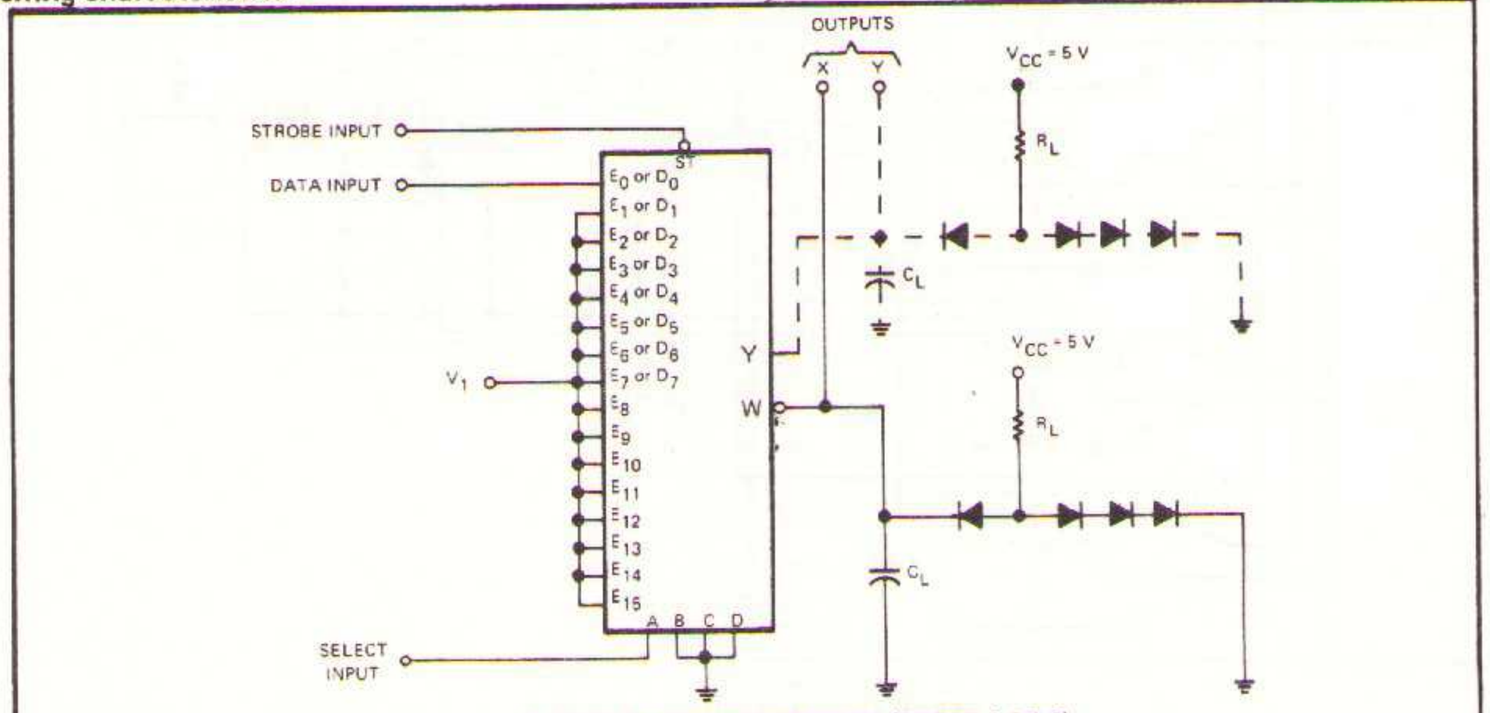
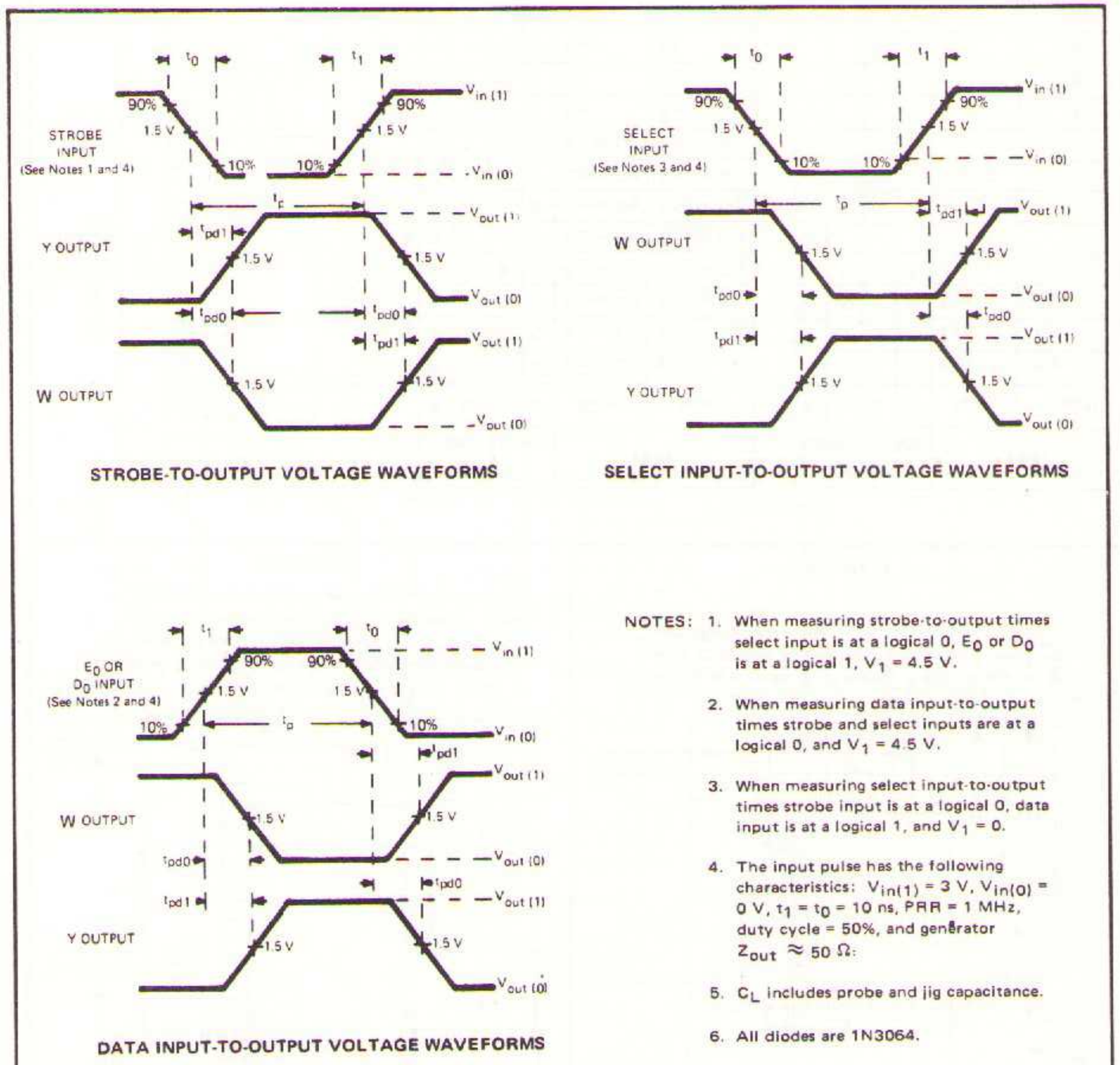


FIGURE 6–SWITCHING TIMES (SHEET 1 OF 2)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES:
1. When measuring strobe-to-output times select input is at a logical 0, E_0 or D_0 is at a logical 1, V_1 = 4.5 V.
2. When measuring data input-to-output times strobe and select inputs are at a logical 0, and V_1 = 4.5 V.
3. When measuring select input-to-output times strobe input is at a logical 0, data input is at a logical 1, and V_1 = 0.
4. The input pulse has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 10 ns, PRR = 1 MHz, duty cycle = 50%, and generator $Z_{out} \approx 50\ \Omega$.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES (SHEET 2 OF 2)

† Tests, as shown, are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Typical Average Propagation Delay Times:

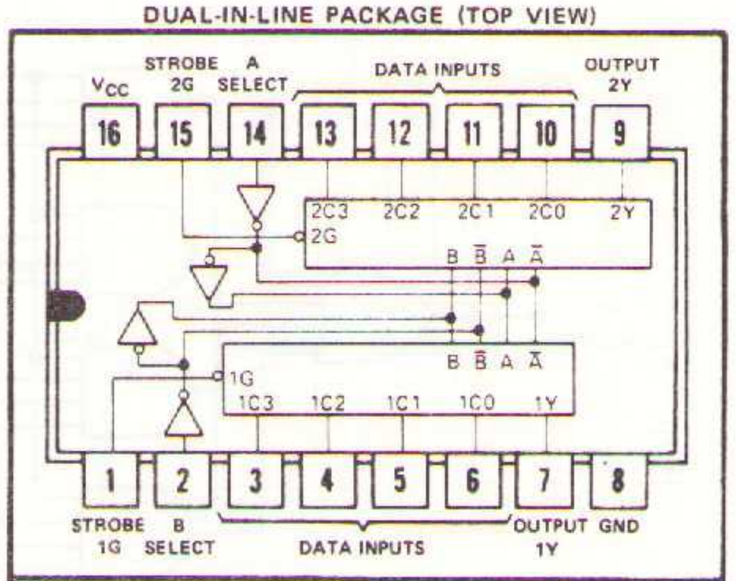
  Data Input to Output . . . . . 14 ns
  Strobe Input to Output . . . . 17 ns
  Select Input to Output . . . . . 22 ns
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Typical power dissipation is 170 milliwatts.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

Resistor values in the OR function have been reduced to values used with Series 54H. This minimizes the capacitive effects of paralleling the phase-splitter transistors and reduces the propagation delay times. The SN54153 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74153 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54153 Circuits . . . . . −55°C to 125°C
SN74153 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54153			SN74153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	Low logic level			10			10	
	High logic level			20			20	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.1		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54153	−20		−55	mA
				SN74153	−18		−57	
I_{CCL}	Supply current, low-level output	5	V_{CC} = MAX	SN54153		36	52	mA
				SN74153		36	60	

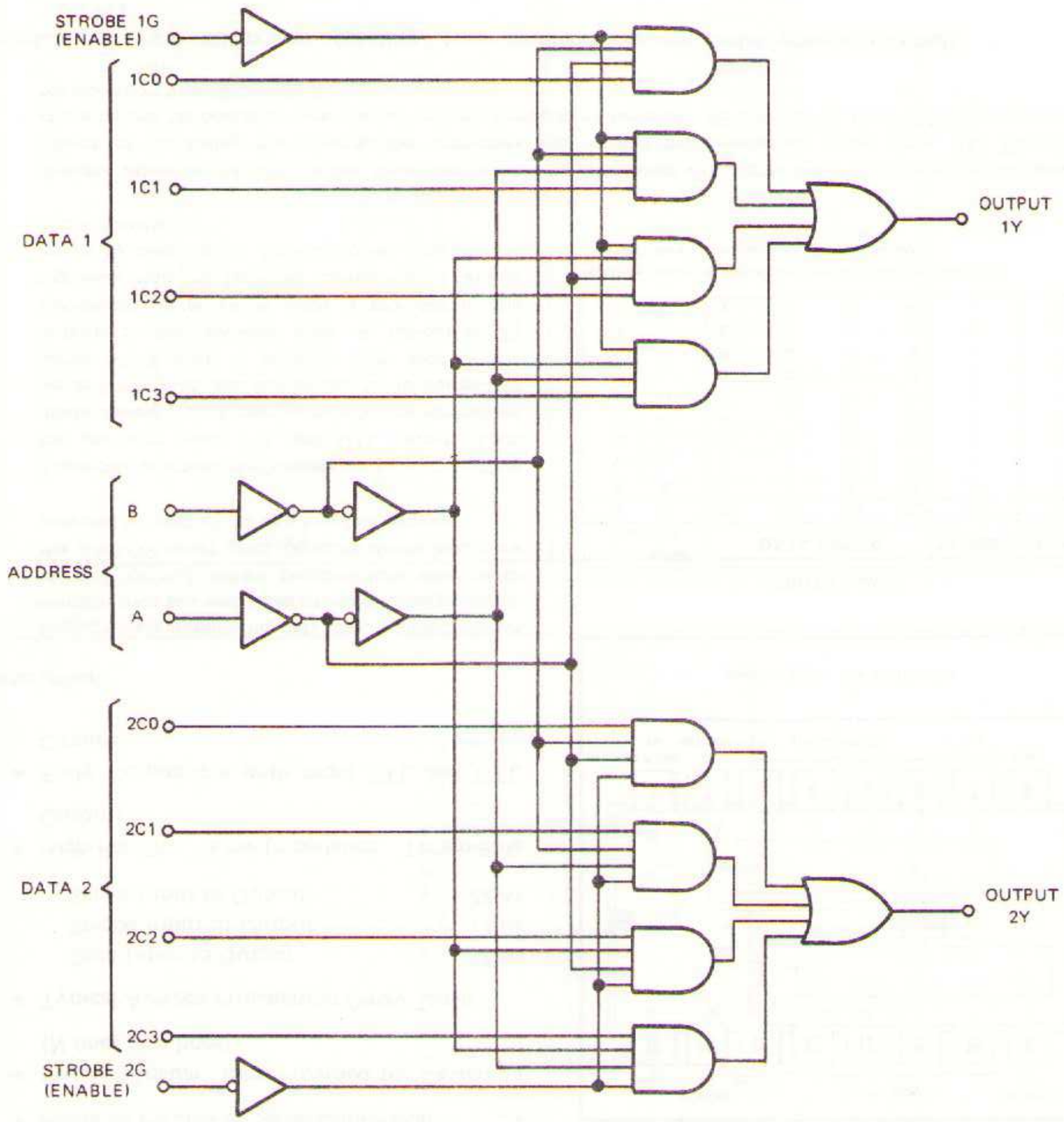
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

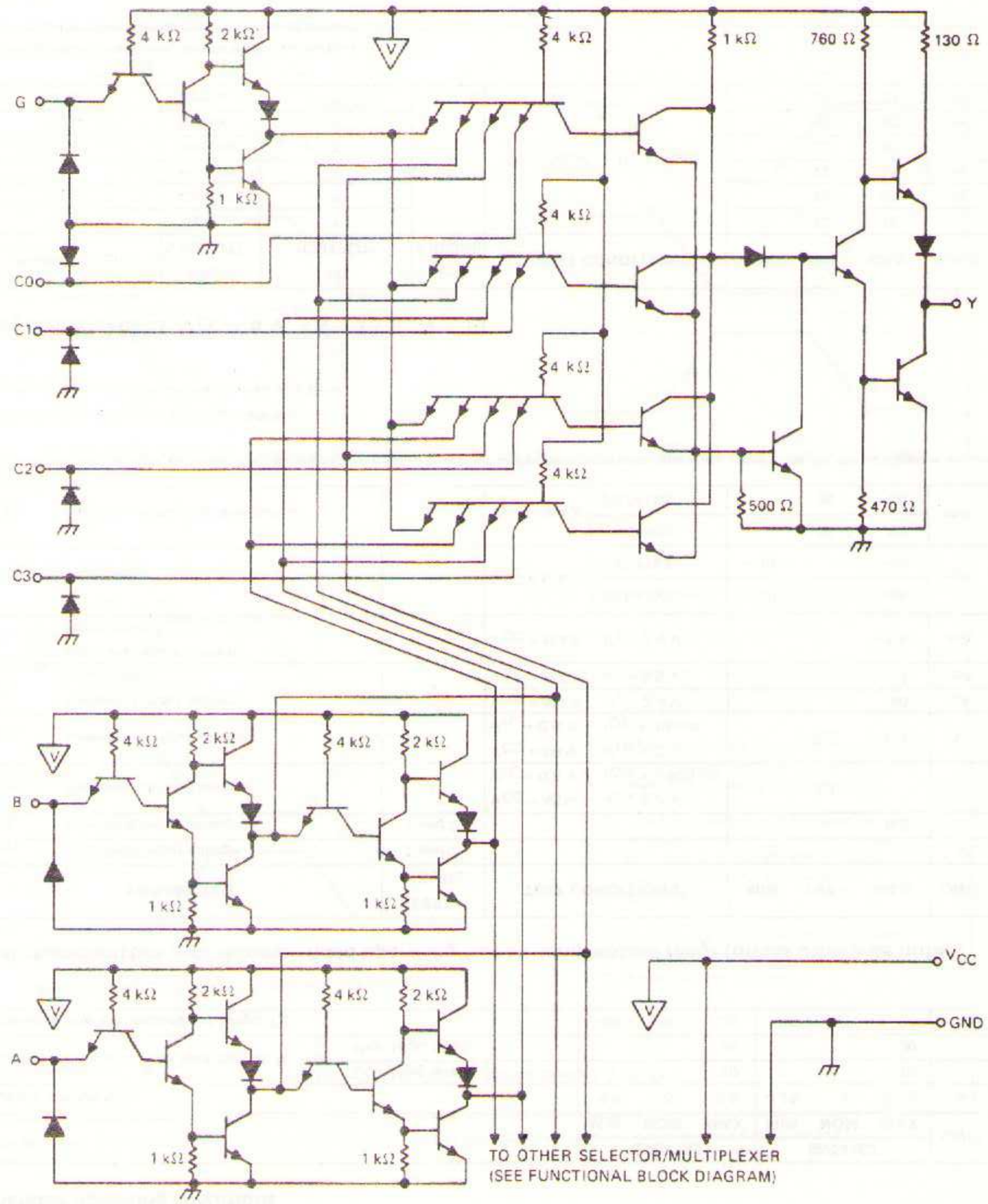
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	6	C_L = 30 pF, R_L = 400 Ω		12	18	
t_{PHL}	Data	Y				15	23	ns
t_{PLH}	Address	Y				22	34	ns
t_{PHL}	Address	Y				22	34	ns
t_{PLH}	Strobe	Y				19	30	ns
t_{PHL}	Strobe	Y				15	23	ns

¶t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

functional block diagram



schematic (each selector/multiplexer, and the common address section)



NOTE: Component values shown are nominal.

V_{CC} bus

d-c test circuits†

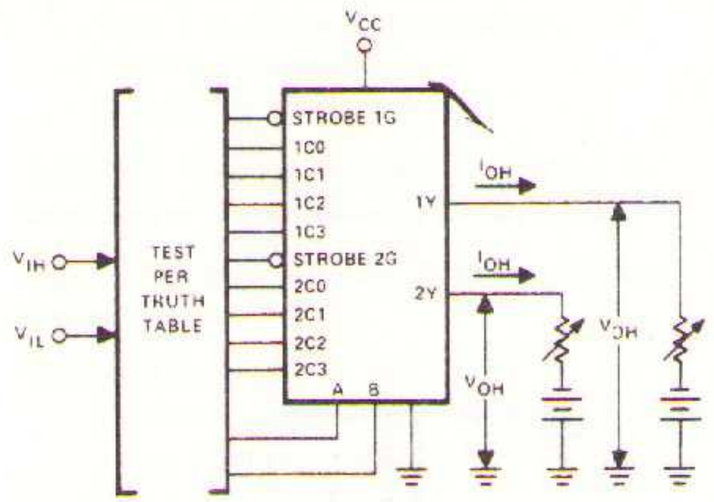


FIGURE 1–V_{IH}, V_{IL}, V_{OH}

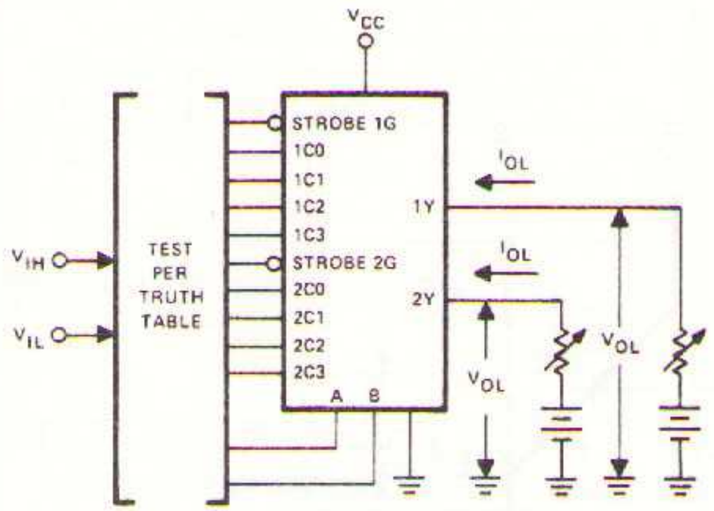
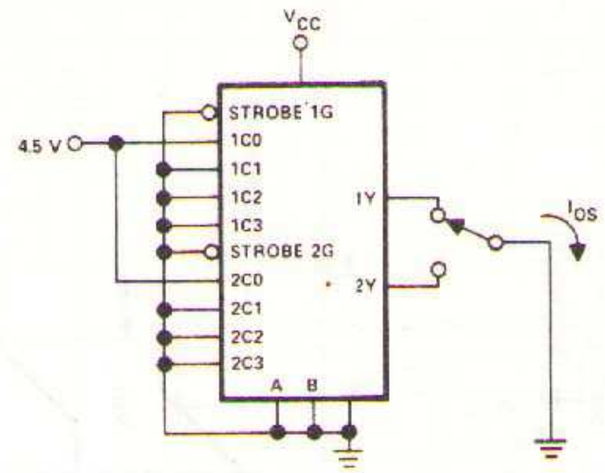


FIGURE 2–V_{IH}, V_{IL}, V_{OL}

d-c test circuits† (continued)



NOTE: Each output is tested separately.

FIGURE 4 – I_{OS}

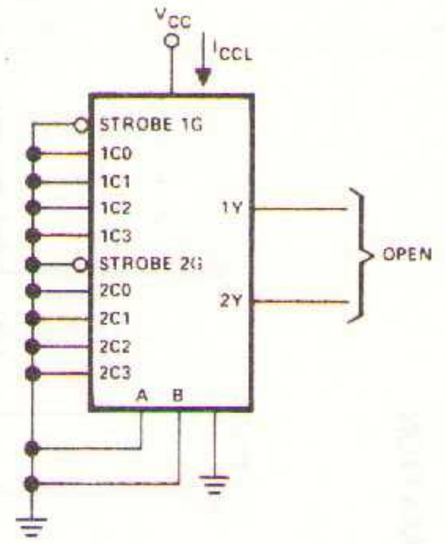
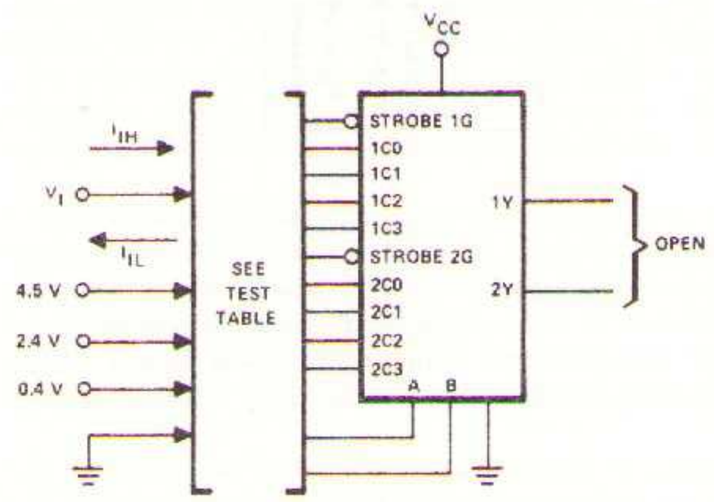


FIGURE 5 – I_{CCL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.



TEST TABLE

INPUT CONDITIONS				APPLY V_I	
B	A	1G	2G	TEST I_{IL}	TEST I_{IH}
L	L	H	H		1C3, 2C3
L	H	H	H		1C2, 2C2
H	L	H	H		1C1, 2C1
H	H	H	H		A, B, 1G, 2G, 1C0, 2C0
L	L	L	L	A, B, 1G, 2G, 1C0, 2C0	
L	H	L	L	1C1, 2C1	
H	L	L	L	1C2, 2C2	
H	H	L	L	1C3, 2C3	

H = 2.4 V, L = 0.4 V

NOTE: Each input is tested separately. When I_{IH} is tested, all C inputs not under test are grounded. When I_{IL} is tested, all C inputs not under test are at 4.5 V.

FIGURE 3 –I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

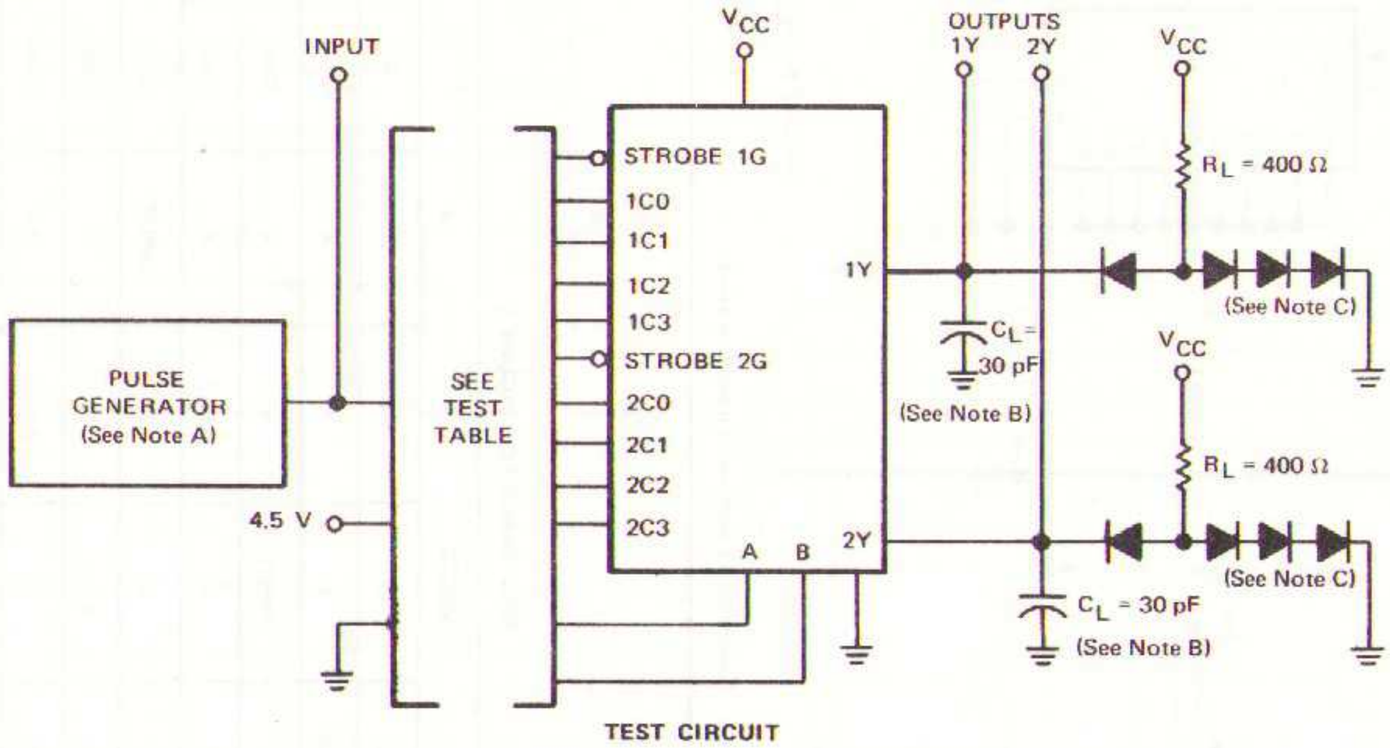
TEST TABLE FOR FIGURE 6

INPUTS							OUTPUT Y WAVEFORM
B	A	C0	C1	C2	C3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5 V	X	INPUT	X	X	GND	A
4.5 V	GND	X	X	INPUT	X	GND	A
4.5 V	4.5 V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5 V	X	X	GND	A
INPUT	GND	GND	X	4.5 V	X	GND	A
GND	GND	4.5 V	X	X	X	INPUT	B

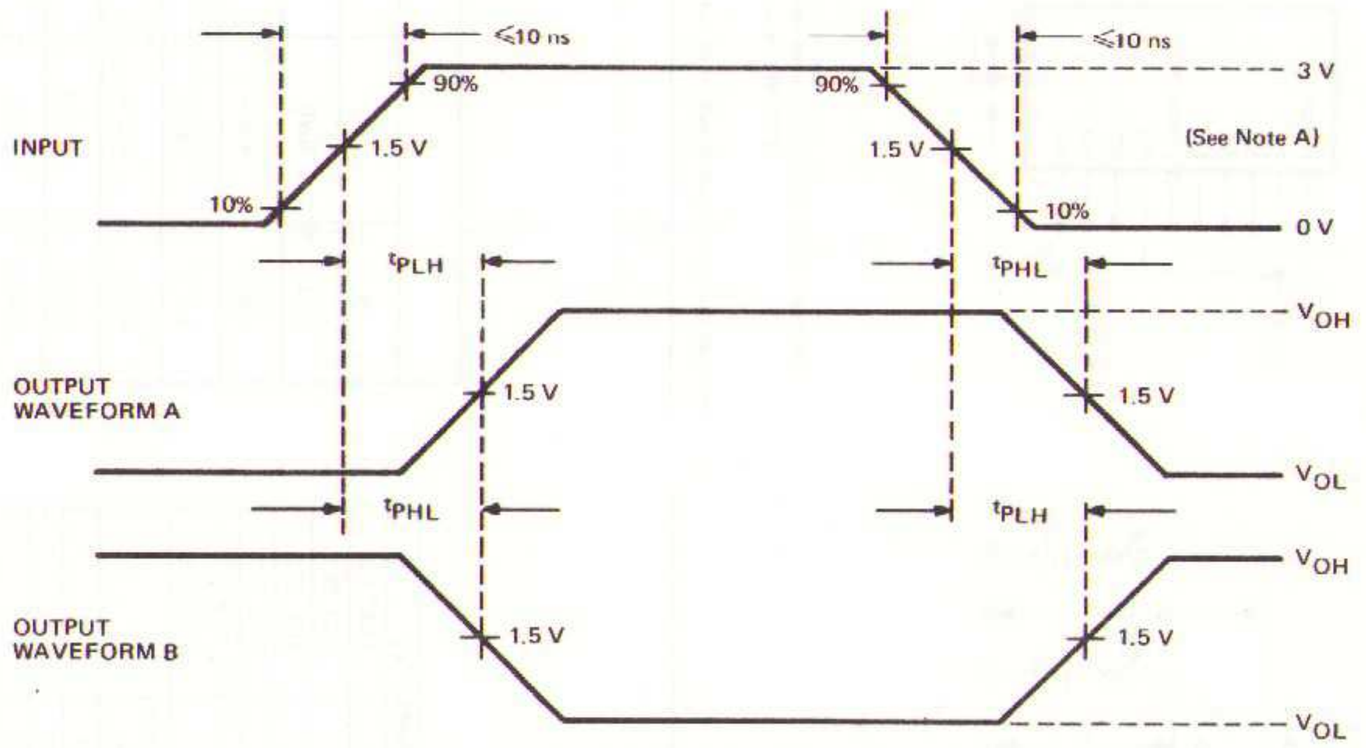
X = irrelevant

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



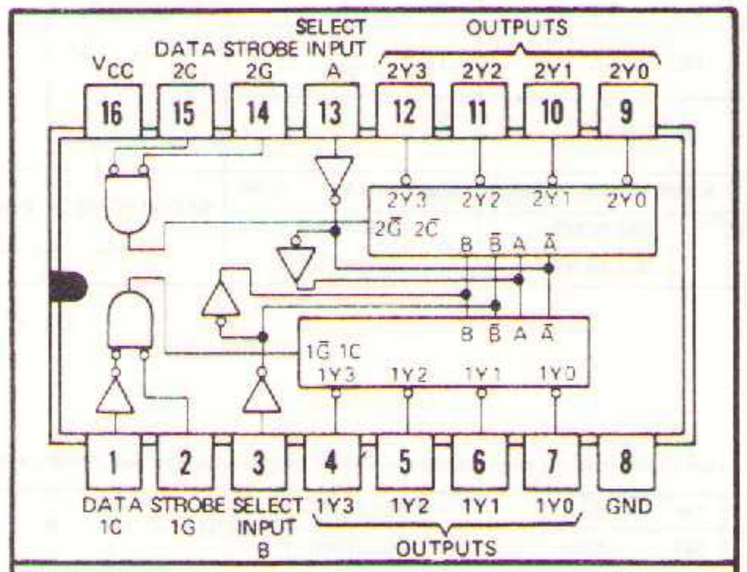
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

- Applications:
  - Dual 2-to-4-Line Decoder
  - Dual 1-to-4-Line Demultiplexer
  - 3-to-8-Line Decoder
  - 1-to-8-Line Demultiplexer
- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Input Clamping Diodes Simplify System Design
- Choice of Outputs:
  - Totem Pole (SN54155, SN74155)
  - Open-Collector (SN54156, SN74156)
- Typical Average Propagation Delay Times:
  - 16 ns through 2 levels of logic
  - 21 ns through 3 levels of logic
- Typical Power Dissipation . . . 125 mW

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: See truth table

description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

The SN54155/SN74155 circuits, with totem-pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The SN54156/SN74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design. Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the SN54155/SN74155.

The SN54155 and SN54156 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74155 and SN74156 are characterized for operation from 0°C to 70°C.

truth tables (H = high level, L = low level, X = irrelevant)

2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE-TO-8-LINE DECODER TO 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54155, SN54156 Circuits . . . . . −55°C to 125°C
SN74155, SN74156 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54155			SN74155			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN54155, SN74155 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX,	V_I = 2.4 V			40	μA
			V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN54155	−20		−55	mA
				SN74155	−18		−57	
I_{CC}	Supply current	6	V_{CC} = MAX	SN54155		25	35	mA
				SN74155		25	40	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN54156, SN74156 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	2 and 3			2			V
V_{IL}	Low-level input voltage	2					0.8	V
I_{OH}	High-level output current	3	V_{CC} = MIN, V_{OH} = 5.5 V	V_I = 2 V,			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX,	V_I = 2.4 V			40	μA
			V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	6	V_{CC} = MAX	SN54156		25	35	mA
				SN74156		25	40	

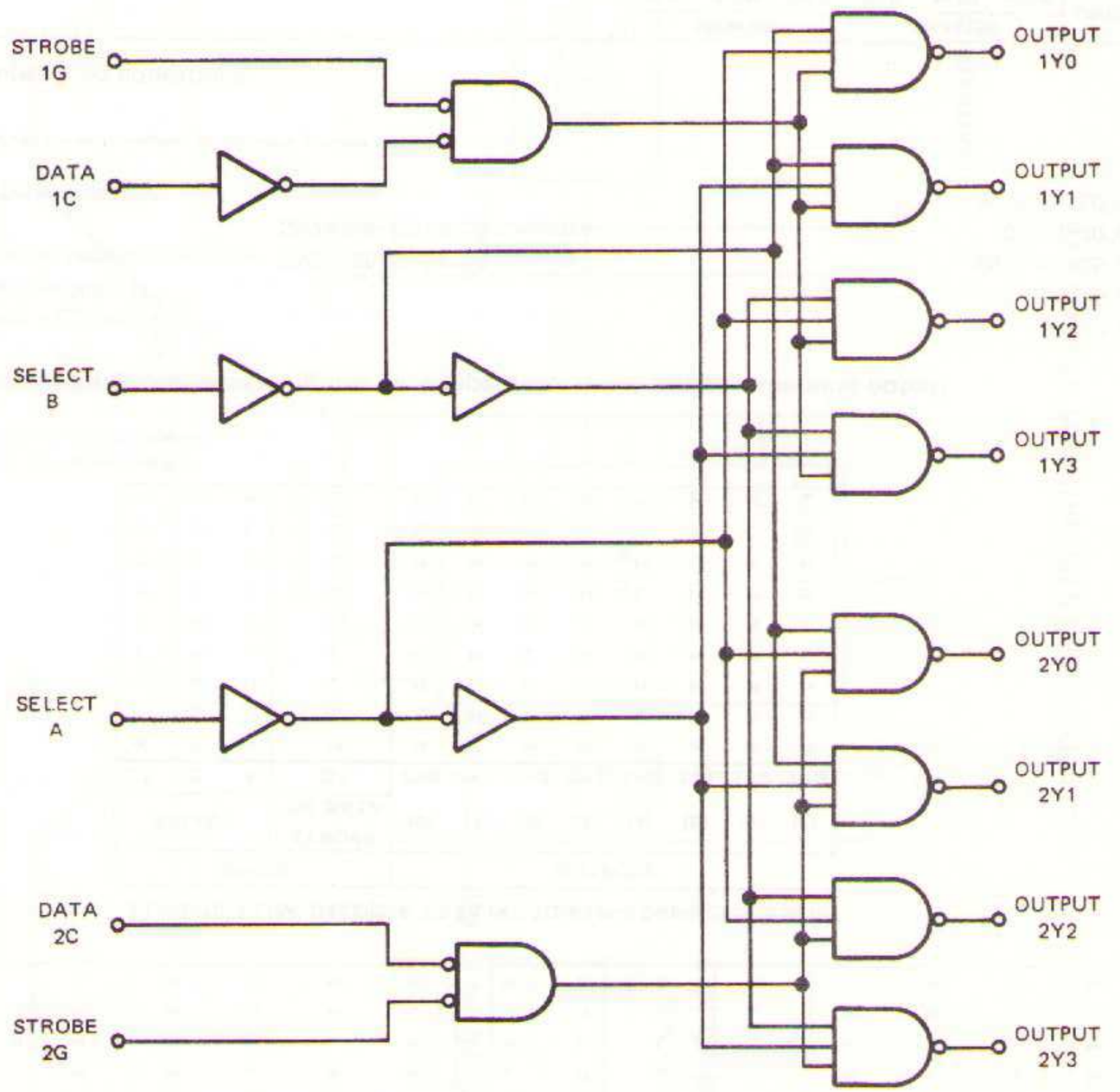
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST FIGURE	TEST CONDITIONS	SN54155 SN74155 MIN	TYP	MAX	SN54156 SN74156 MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	7	C_L = 15 pF, R_L = 400 Ω		13	20		15	23	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2				18	27		20	30	ns
t_{PLH}	A or B	Y	3				21	32		23	34	ns
t_{PHL}	A or B	Y	3				21	32		23	34	ns
t_{PLH}	1C	Y	3				16	24		18	27	ns
t_{PHL}	1C	Y	3				20	30		22	33	ns

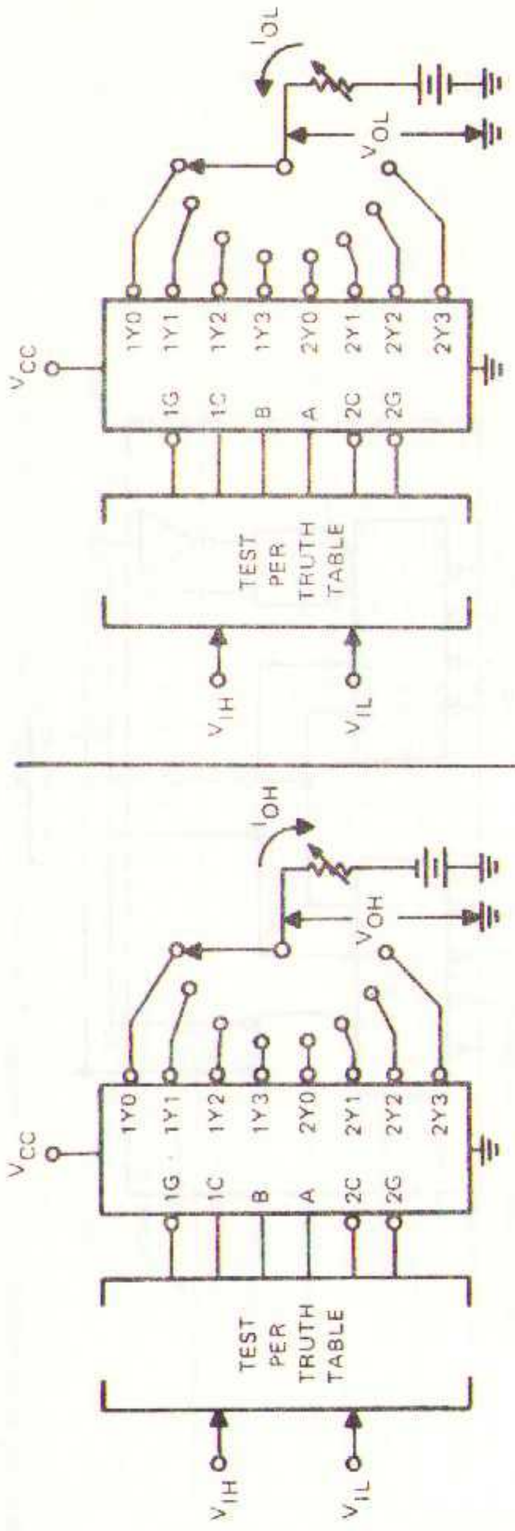
¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

functional block diagram



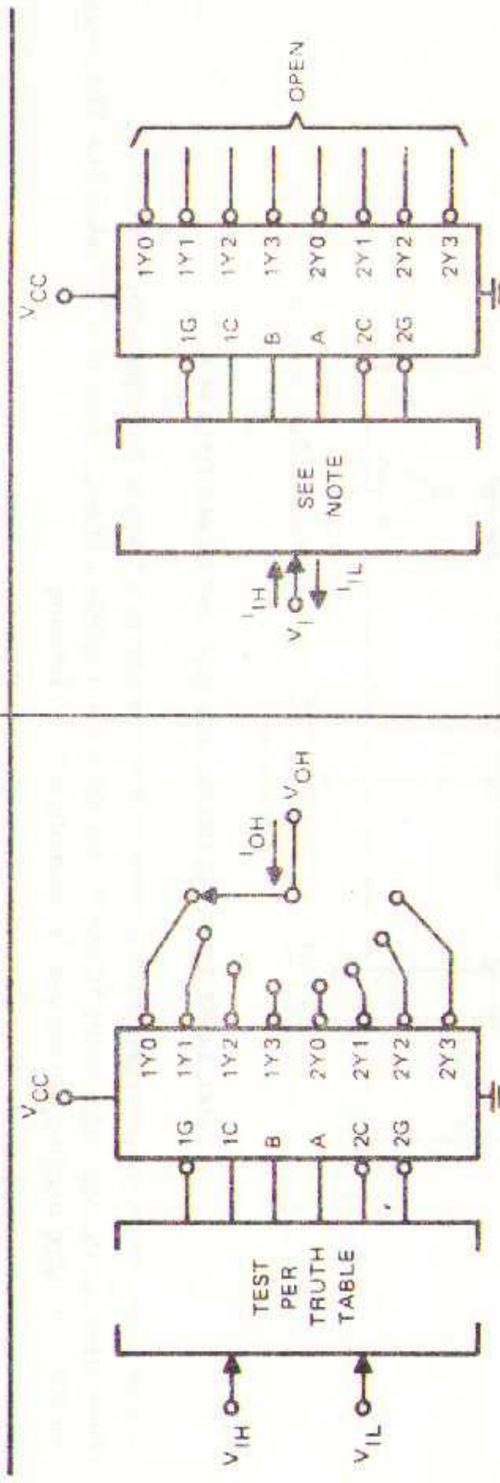
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

FIGURE 3–V_{IH}, V_{IL}, I_{OH}

Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

Each input is tested separately for both I_{IH} and I_{IL}. Inputs not under test are grounded.

FIGURE 4–I_{IH}, I_{IL}

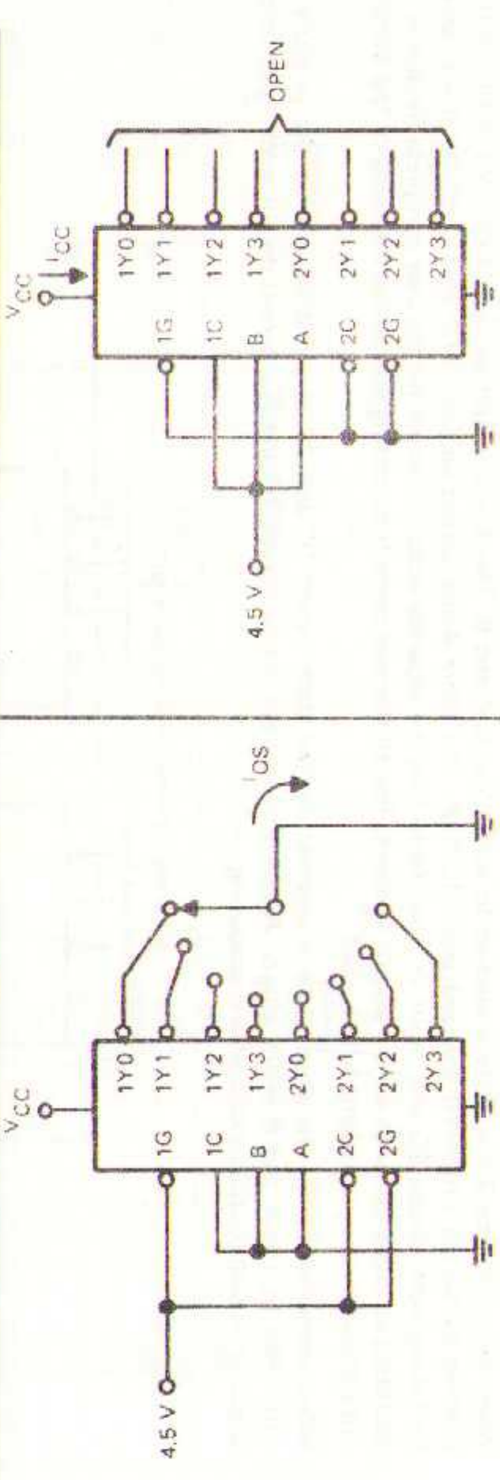


FIGURE 6–I_{CC}

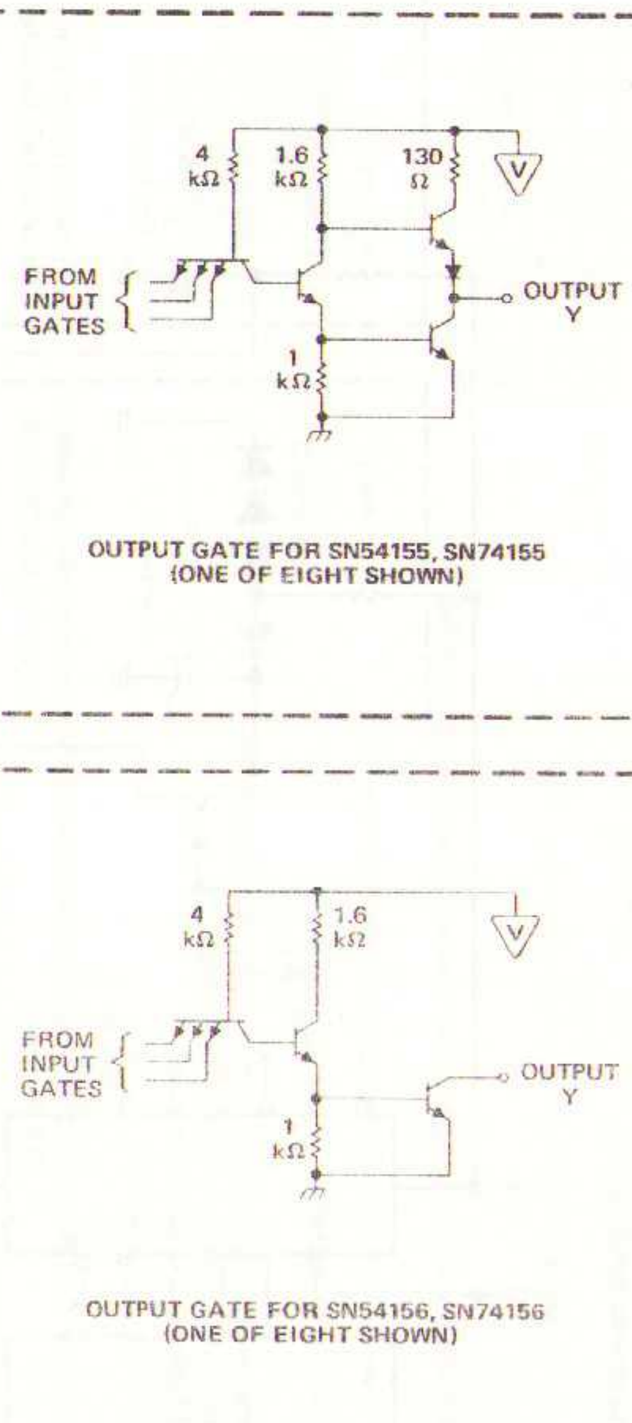
Each output is tested separately.

FIGURE 5–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

ADDRESS INPUT GATES FOR SN54155, SN54156, SN74155, SN74156

OUTPUT GATE FOR SN54155, SN74155
(ONE OF EIGHT SHOWN)



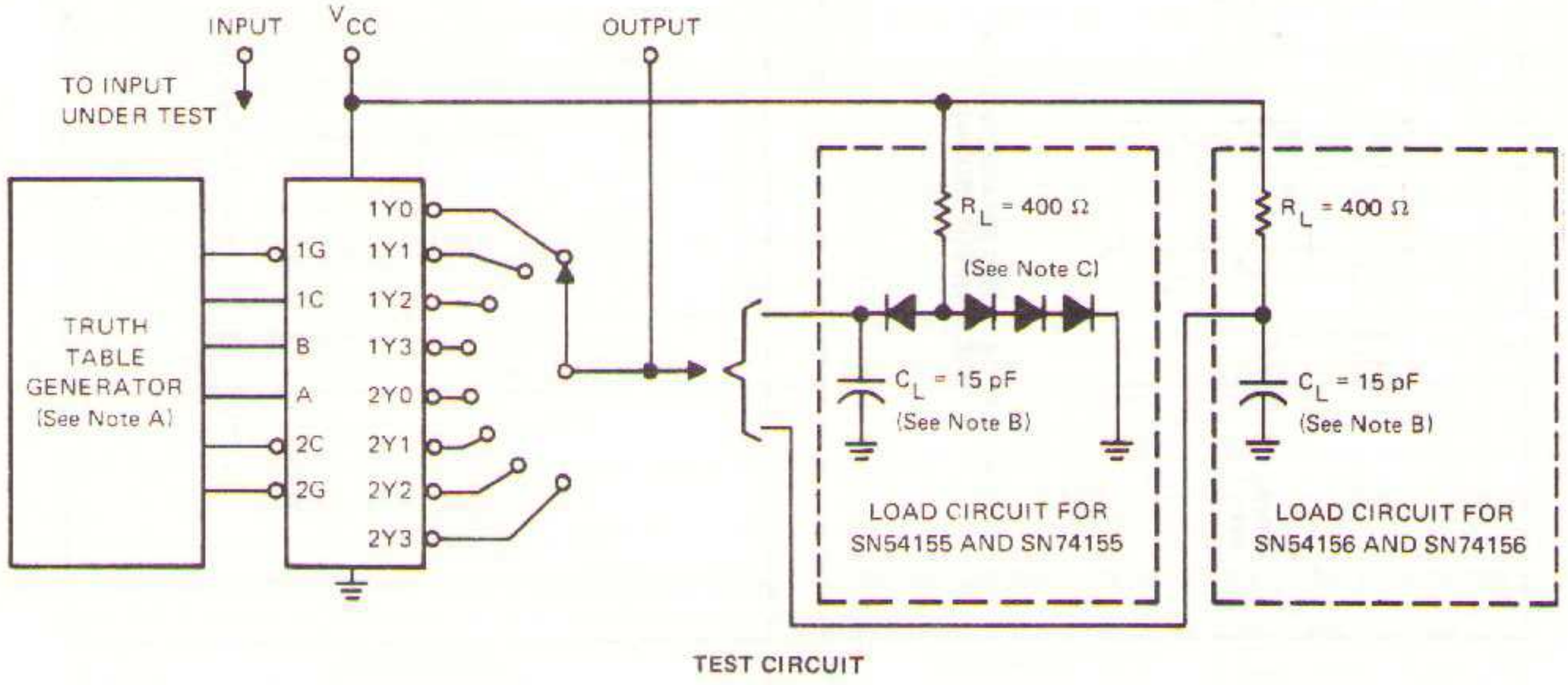
OUTPUT GATE FOR SN54156, SN74156
(ONE OF EIGHT SHOWN)

Component values shown are nominal.

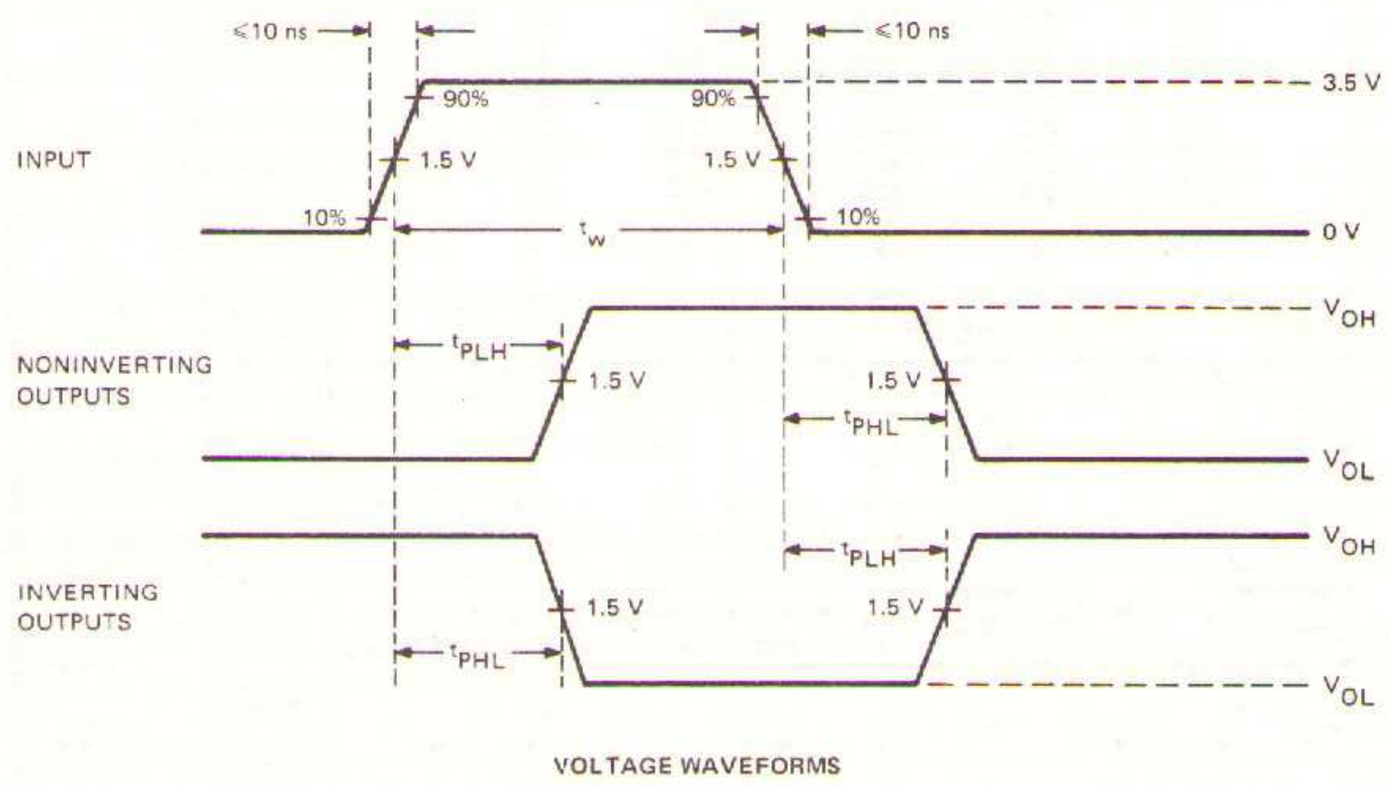
V V_{CC} bus

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The truth table generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

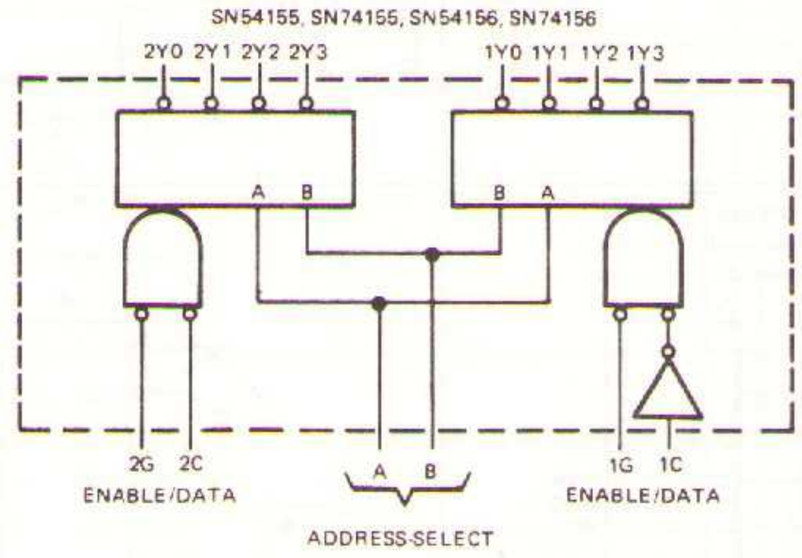
FIGURE 7—PROPAGATION DELAY TIME

TYPICAL APPLICATION DATA

THE SN54155, SN74155, SN54156, or SN74156 may be used as a dual 2-line-to-4-line decoder or a 1-line-to-4-line demultiplexer. These applications are identical except as follows:

When decoding, the 2-line code is applied to select inputs A and B. The 4-line output section (1Y0, 1Y1, 1Y2, 1Y3) is enabled by taking strobe 1G low and input 1C high. The other 4-line output section (2Y0, 2Y1, 2Y2, 2Y3) is enabled by taking both strobe 2G and input 2C low. Note that the separate enable lines permit the user complete flexibility in decoding at either or both of the output sections. The strobe also permits cascading and allows disabling of the circuits until the addressing transients have passed.

When demultiplexing, the serial data is applied to the data inputs 1C and 2C and distribution to the outputs is controlled by the A and B select inputs. Again, the separate strobe inputs, 1G and 2G, permit demultiplexing to occur at either or both output sections, and cascading.

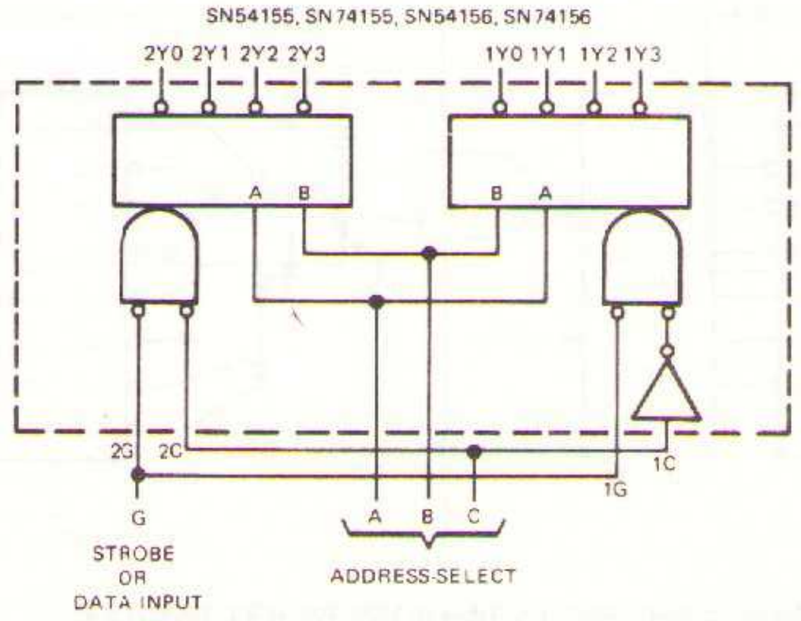


DUAL 2-LINE-TO-4-LINE DECODER/1-TO-4-LINE DEMULTIPLEXER

Any of these circuits may also be used as a 3-line-to-8-line decoder or a 1-line-to-8-line demultiplexer.

When used as a decoder, data inputs 1C and 2C are connected together and serve as the third (C) select line. The strobes are also connected together and are used for enabling and/or cascading.

When used as a demultiplexer, the common strobe line serves as the data input.



3-LINE-TO-8-LINE DECODER/1-TO-8-LINE DEMULTIPLEXER

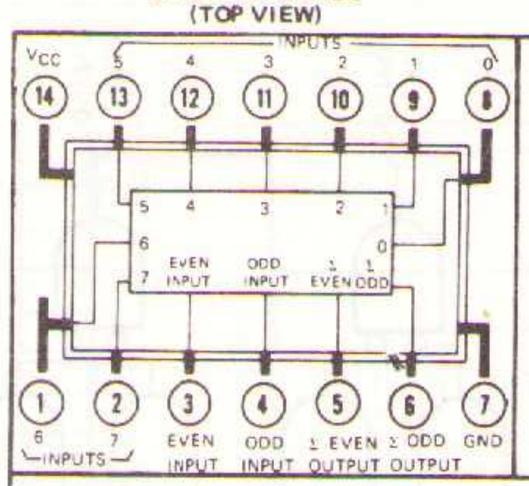
logic

TRUTH TABLE

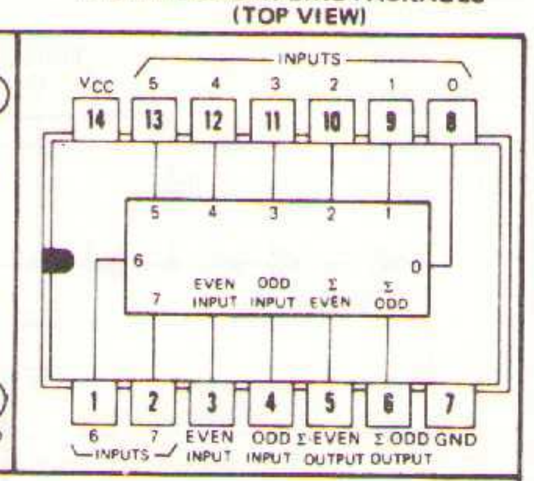
INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

S FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGES (TOP VIEW)



positive logic: see truth table

description

These universal, monolithic, 8-bit parity generators/checkers, utilizing familiar Series 54/74 TTL circuitry, feature odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications. The word-length capability is easily expanded by cascading. Typical applications are shown for these parity circuits being used to generate and check parity.

The SN54180/74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized loads is provided in the logical 1 state to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74180 is characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Case Temperature Range, SN54180S . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN54180J, SN54180N . . . . . −55°C to 125°C
SN74180 . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN54180	4.5	5	5.5	V
	SN74180	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	V
	Logical 1			20	V

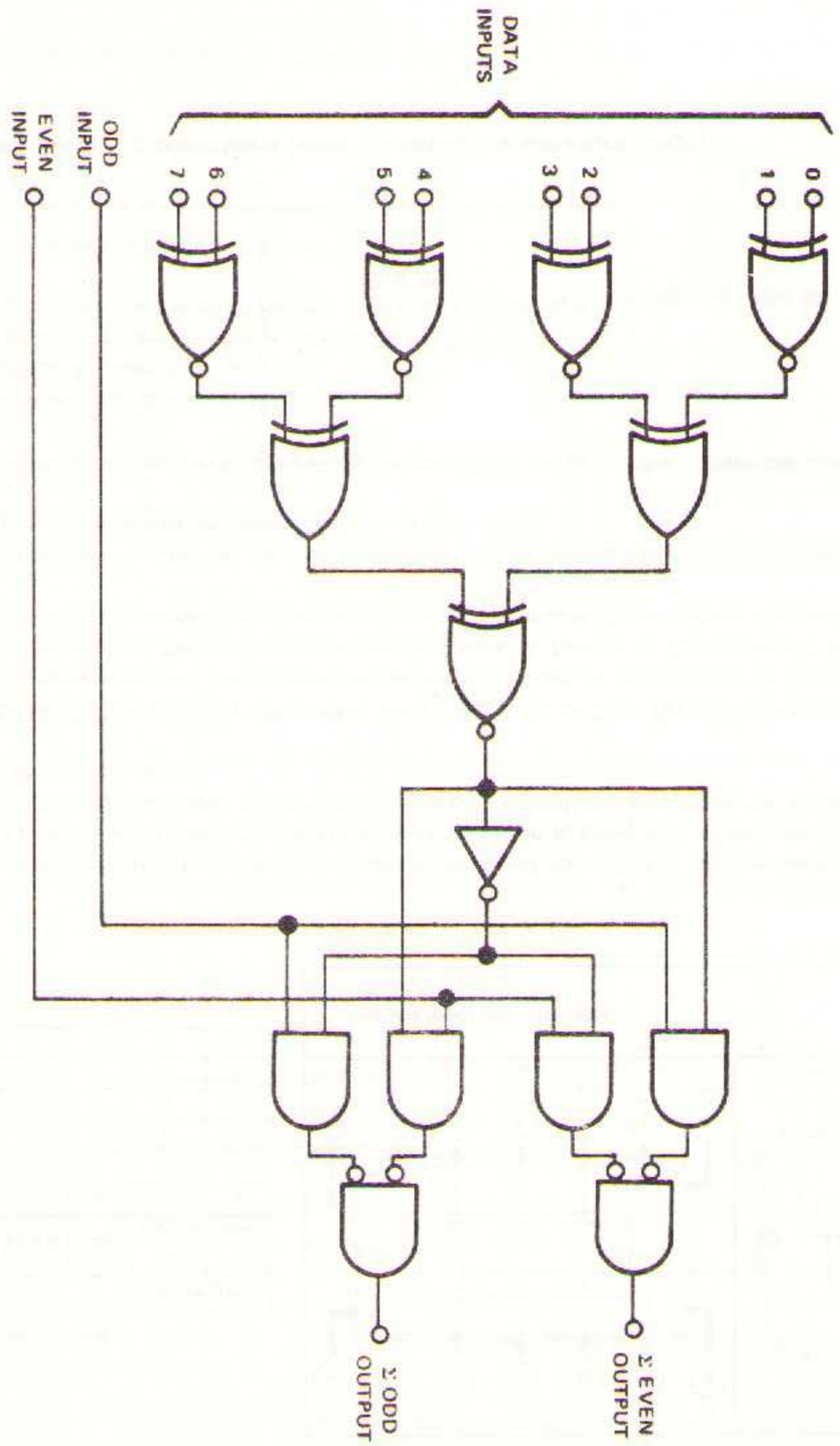
electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at each data input	2	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at each data input	2	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
I_{OS}	Short circuit output current§	3	V_{CC} = MAX	SN54180	−20		−55	mA
				SN74180	−18		−55	mA
I_{CC}	Supply current	3 and 4	V_{CC} = MAX	SN54180		34	49	mA
				SN74180		34	56	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω		25	38	ns
t_{pd1}	Data	Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		25	38	ns
t_{pd1}	Even or Odd	Σ Even or Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		13	20	ns
t_{pd0}	Even or Odd	Σ Even or Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		7	10	ns



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

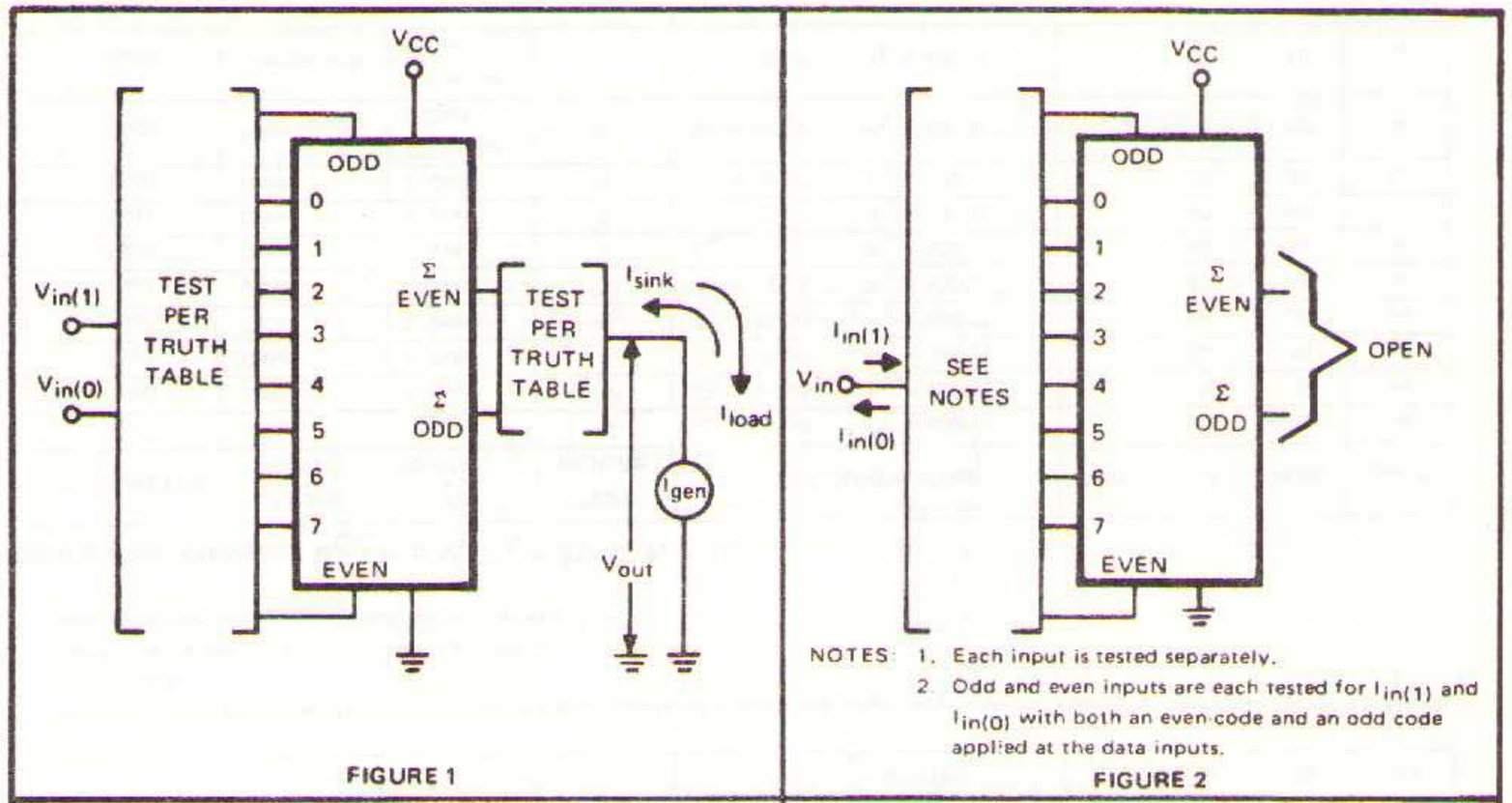
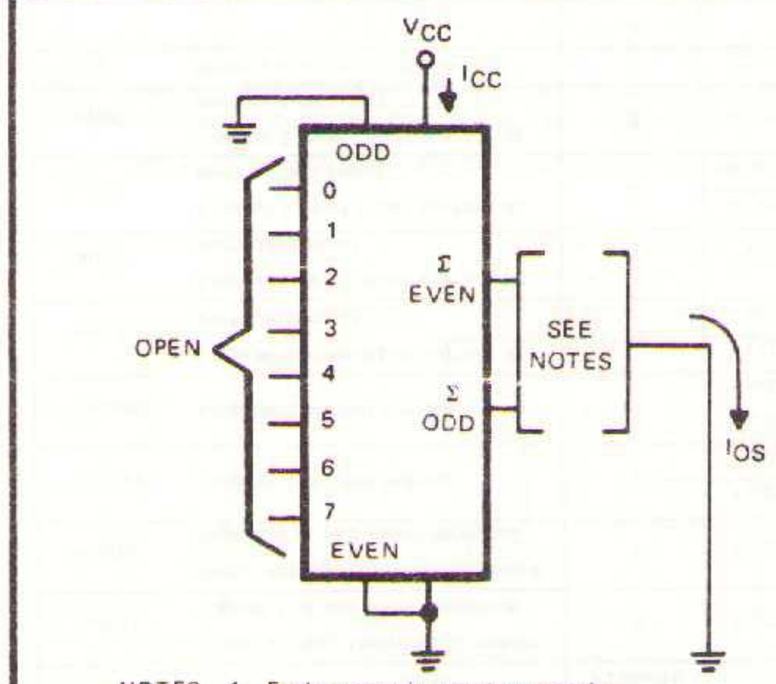


FIGURE 1

NOTES: 1. Each input is tested separately.
2. Odd and even inputs are each tested for $I_{in(1)}$ and $I_{in(0)}$ with both an even code and an odd code applied at the data inputs.

FIGURE 2



NOTES: 1. Each output is tested separately.
2. When testing I_{CC} both outputs are open.

FIGURE 3

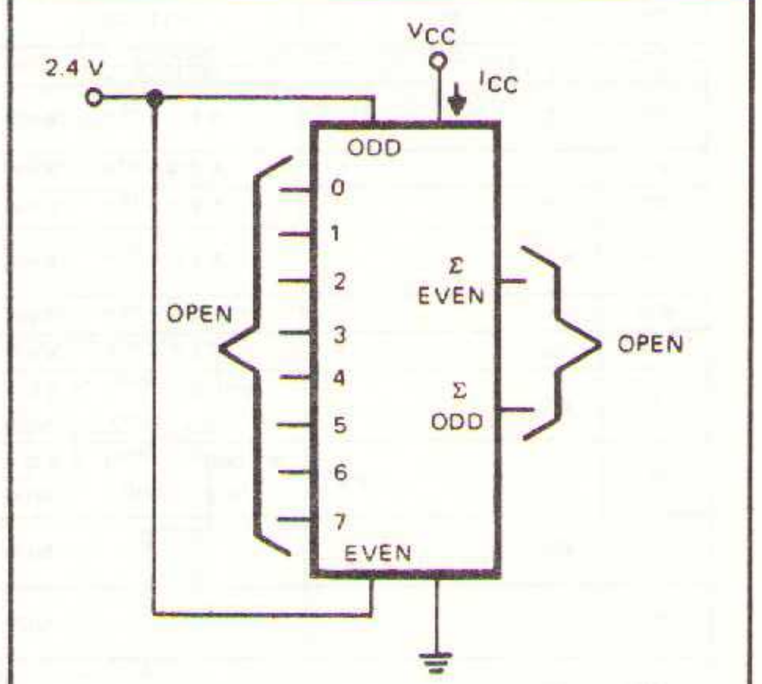
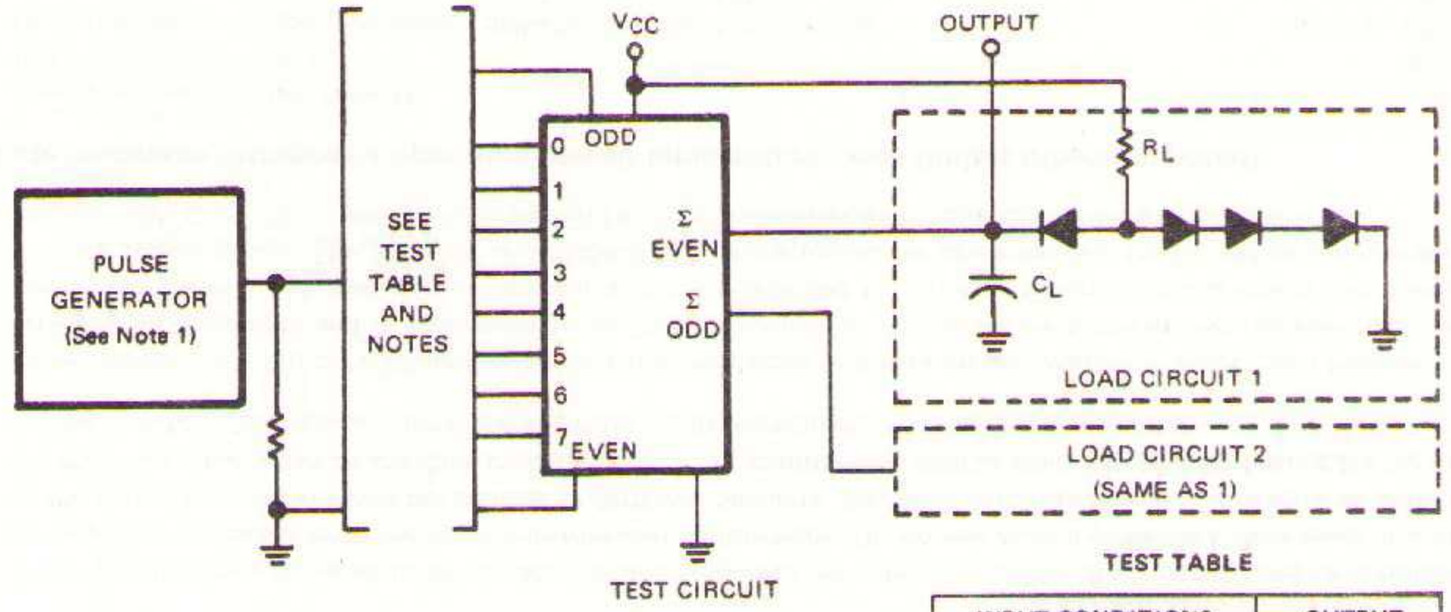


FIGURE 4

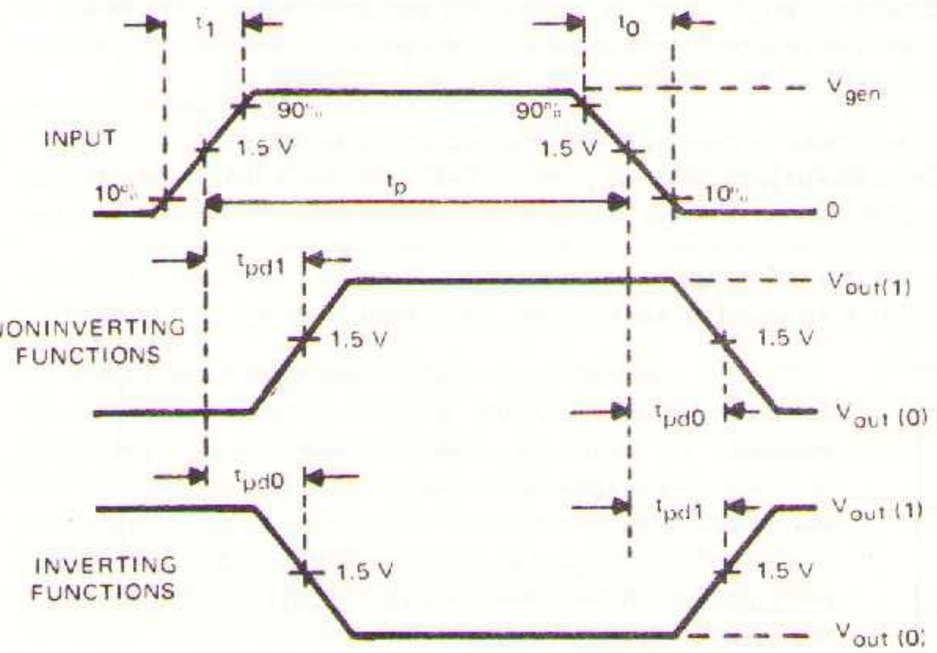
†Arrows indicate actual direction of current flow.

switching characteristics



TEST TABLE

INPUT CONDITIONS		OUTPUT
PULSE	GND	TESTED
0	ODD	Σ EVEN
1	ODD	Σ EVEN
2	ODD	Σ EVEN
3	ODD	Σ EVEN
4	ODD	Σ EVEN
5	ODD	Σ EVEN
6	ODD	Σ EVEN
7	ODD	Σ EVEN
0	ODD	Σ ODD
1	ODD	Σ ODD
2	ODD	Σ ODD
3	ODD	Σ ODD
4	ODD	Σ ODD
5	ODD	Σ ODD
6	ODD	Σ ODD
7	ODD	Σ ODD
EVEN	NONE	Σ EVEN
ODD	0	Σ EVEN
EVEN	0	Σ ODD
ODD	NONE	Σ ODD



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0 = 10$ ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.

FIGURE 5 – SWITCHING TIMES

verifying transmitted data

In this example (Figure A), data is being transmitted from data register A to data register B. Parity generators A1 and A2 are connected to generate an even-parity bit Q_{16} which is transmitted to register B. Parity checkers B1 and B2 verify the accuracy of the transmitted data and generate an even true (logical 1) or false (logical 0) parity output signal.

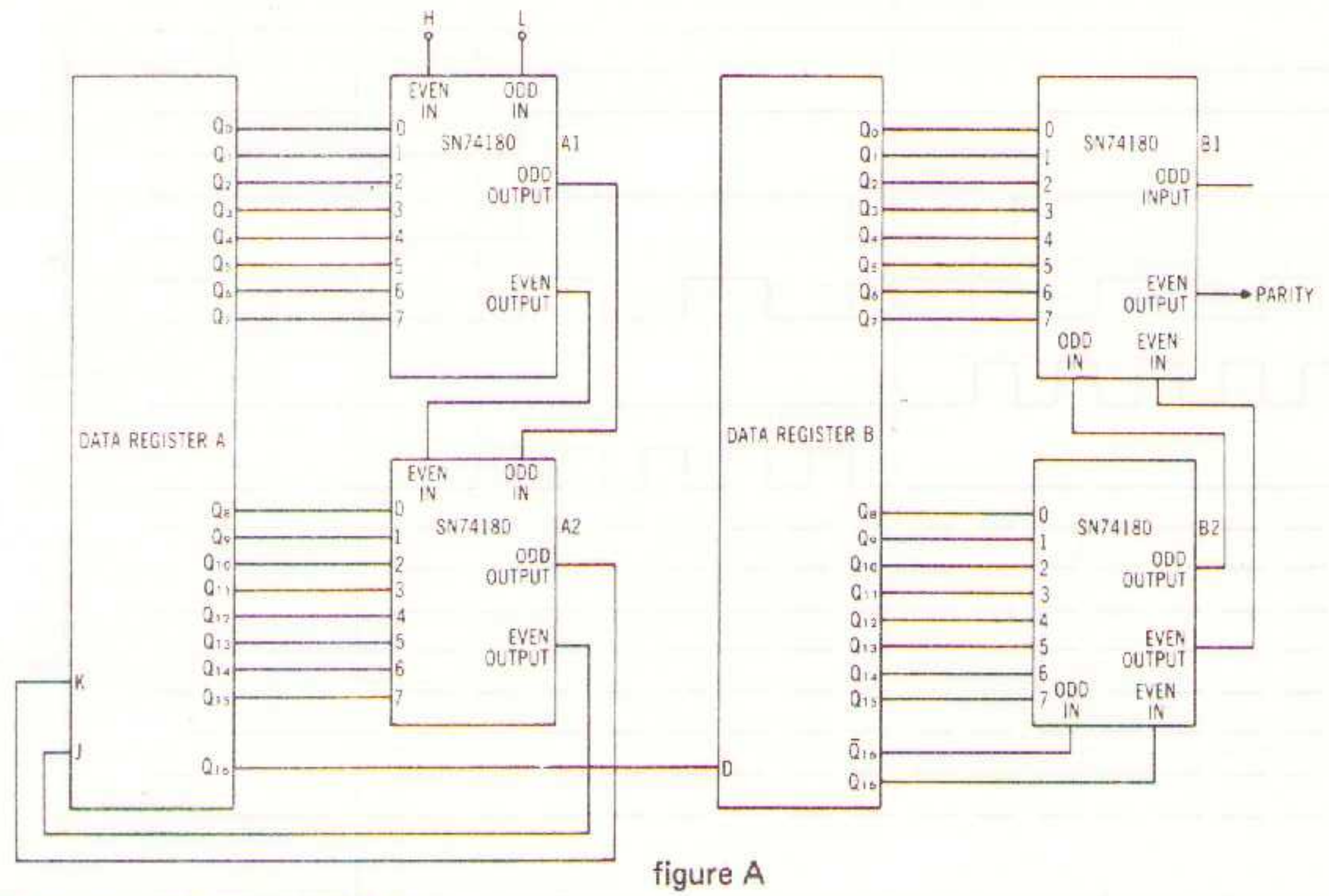


figure A

cascading for longer word lengths

The parity generator/checker may be cascaded for applications requiring longer word lengths. See Figure B. The ODD IN control is grounded for even parity generation and the EVEN IN control is grounded for odd parity generation. Two control inputs and two outputs ensure faster operation when cascading for word lengths over 8 bits, as only one gate delay is added for each additional 8-bit group. For a 32-bit word, parity can be generated in approximately 65 ns.

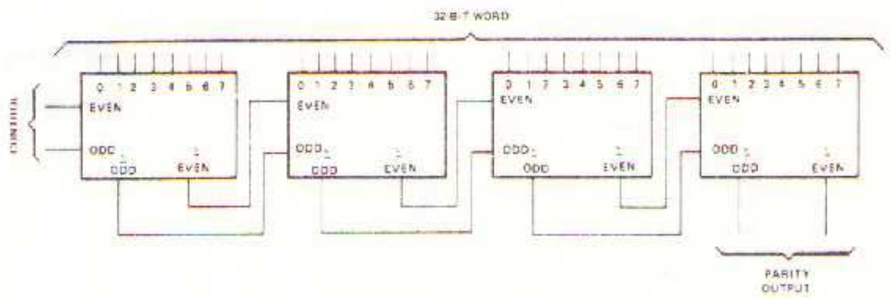
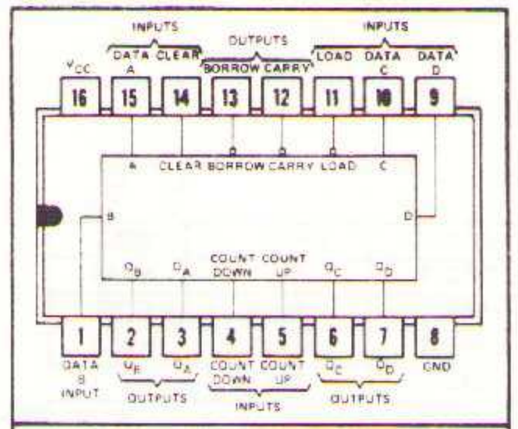


figure B

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input
- Typical Maximum Input Count Frequency . . . 32 MHz

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The SN54192 and SN74192 are BCD counters and the SN54193 and SN74193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input count frequency is typically 32 megahertz and is guaranteed to be 25 MHz minimum. All inputs are buffered and represent only one normalized Series 54/74 load. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. The SN54192 and SN54193 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74192 and SN74193 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Operating free-air temperature range: SN54192 and SN54193 Circuits	−55°C to 125°C
SN74192 and SN74193 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

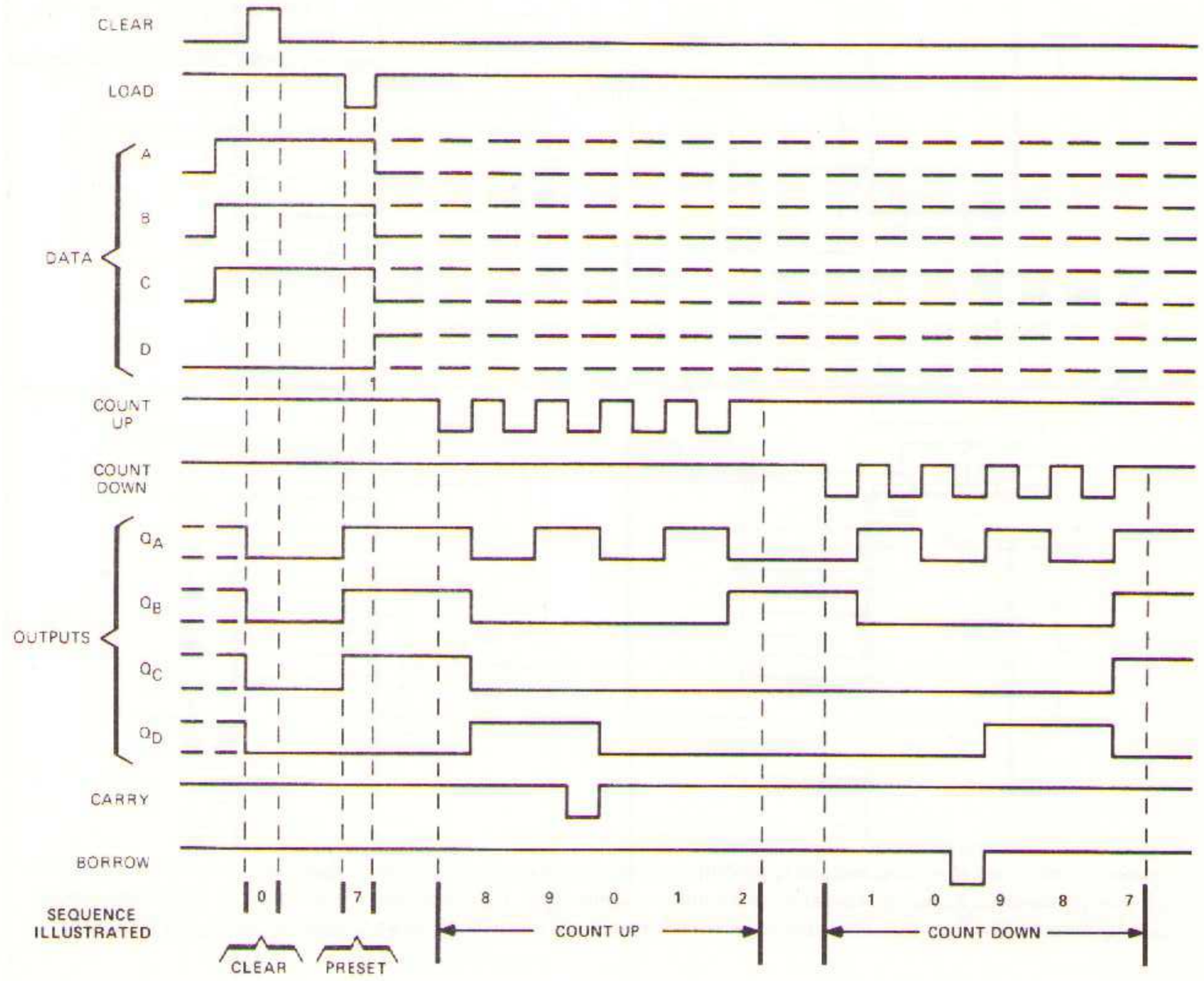
NOTE 1: Voltage values are with respect to network ground terminal.

SN54192, SN74192 DECADE COUNTER

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.

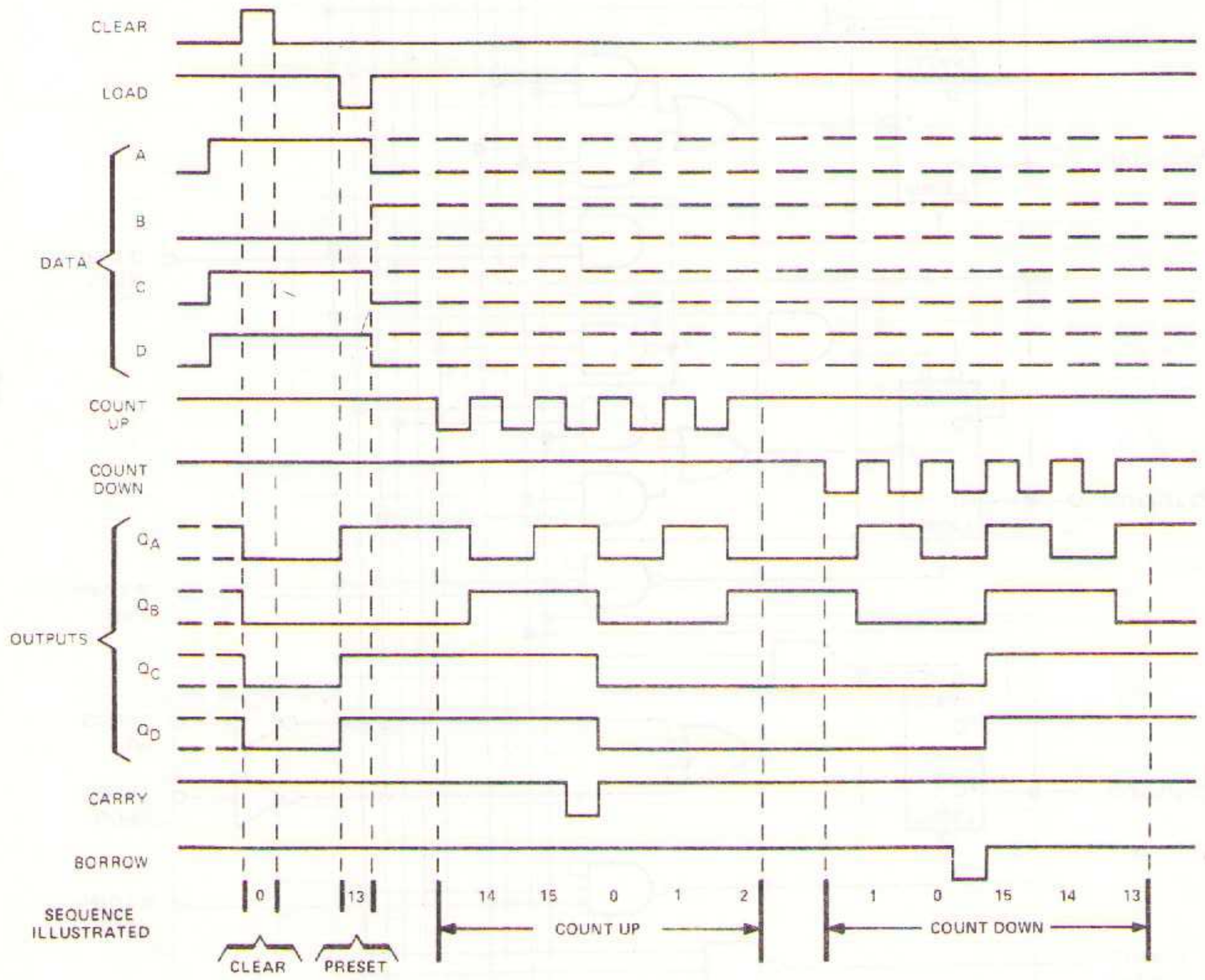


NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high, when counting down, count-up input must be high.

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

recommended operating conditio

	SN54192, SN54193			SN74192, SN74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Input count frequency, f_{count}	0		25◊	0		25◊	MHz
Width of any input pulse, t_w	20◊			20◊			ns
Data setup time, t_{setup} (see Figure 7 and Note 2)	20◊			20◊			ns
Data hold time, t_{hold} (see Note 3)	0			0			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

NOTES: 2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

◊These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	SN54192, SN54193			SN74192, SN74193			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1 and 2		2			2			V
V_{IL}	Low-level input voltage	1 and 2				0.8			0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	6	V_{CC} = MAX		65	89		65	102	mA

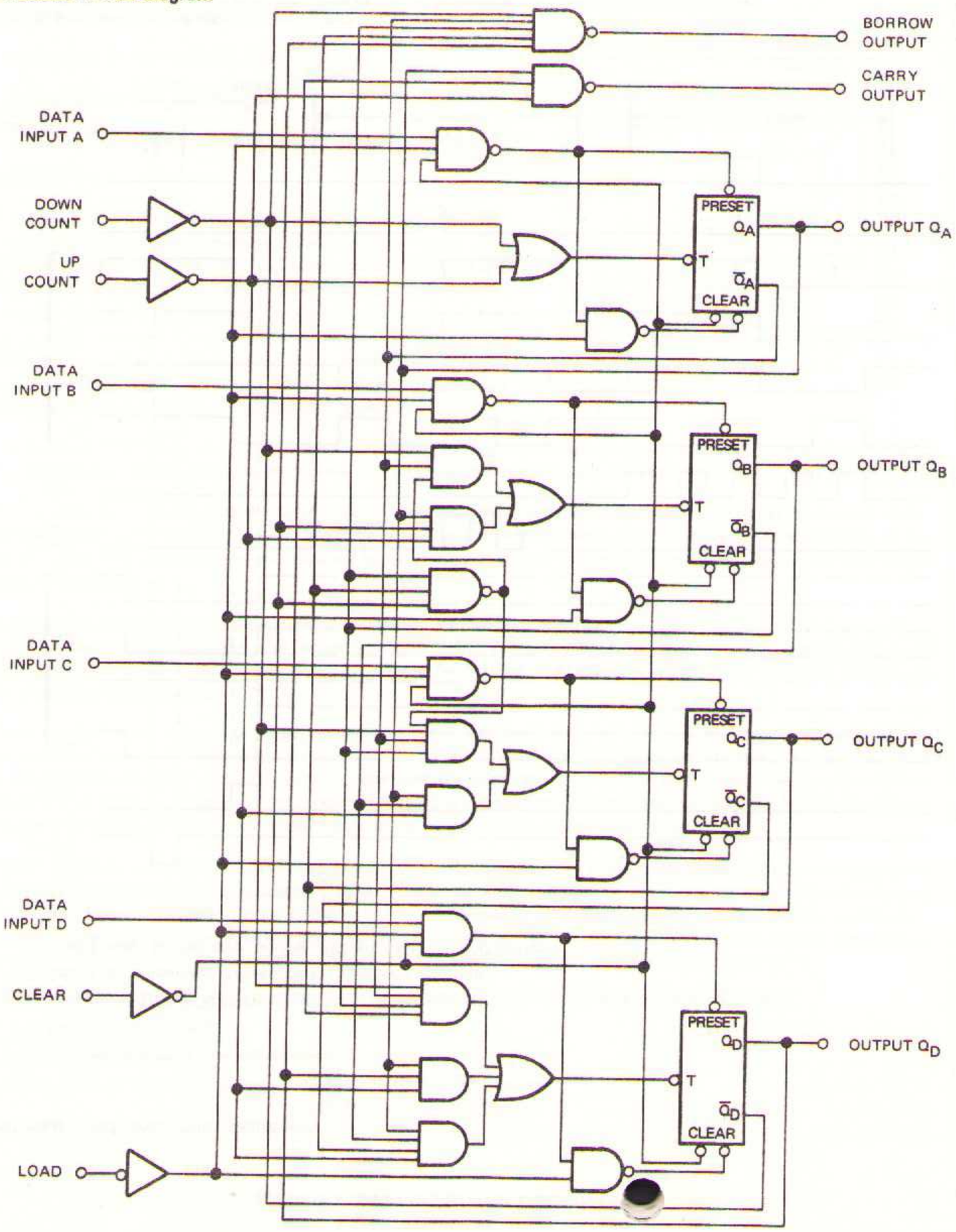
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency		C_L = 15 pF, R_L = 400 Ω	25	32		MHz
t_{setup}	Minimum input setup time	7			14	20	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from count-up input	8			17	26	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from count-up input				16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level borrow output from count-down input				16	24	ns
t_{PHL}	Propagation delay time, high-to-low-level borrow output from count-down input				16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from either count input				25	38	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from either count input				31	47	ns

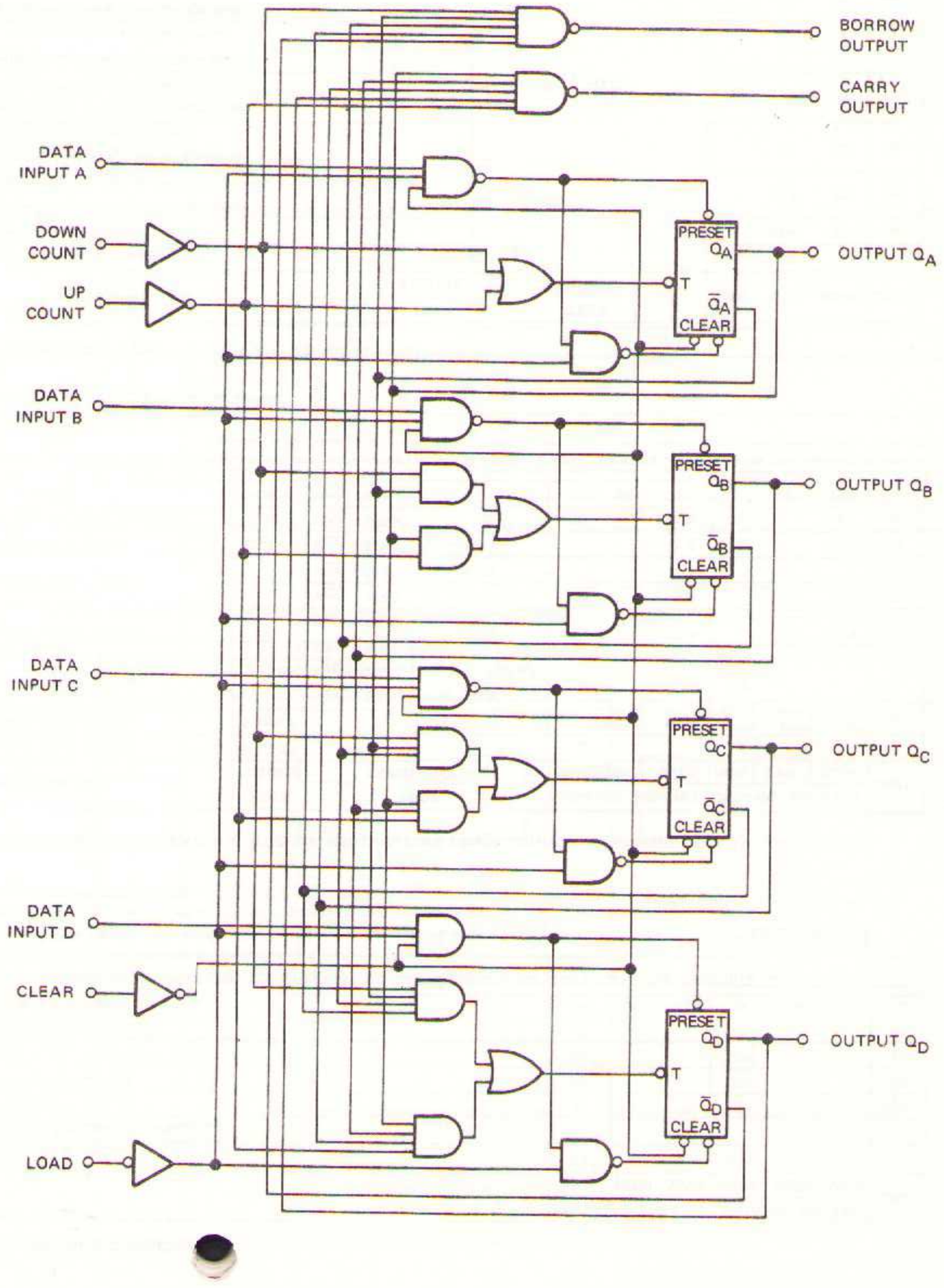
SN54192, SN74192 DECADE COUNTER

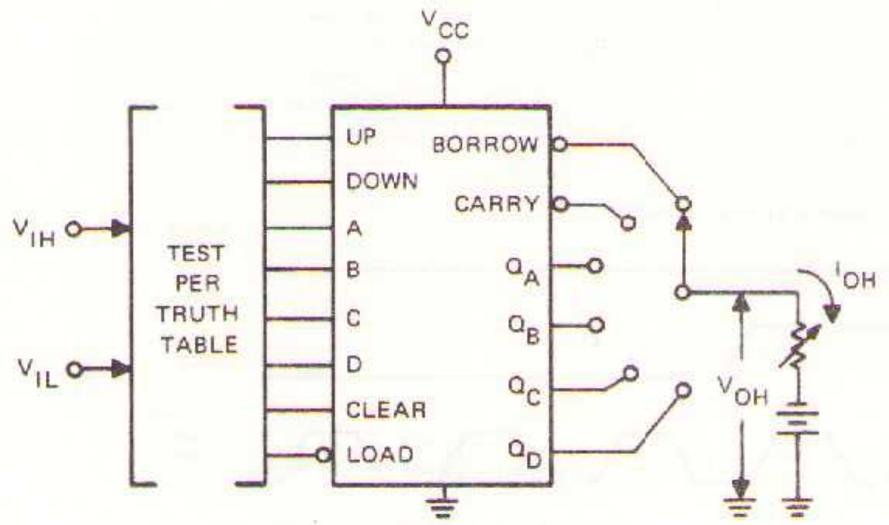
functional block diagram



SN54193, SN74193 BINARY COUNTER

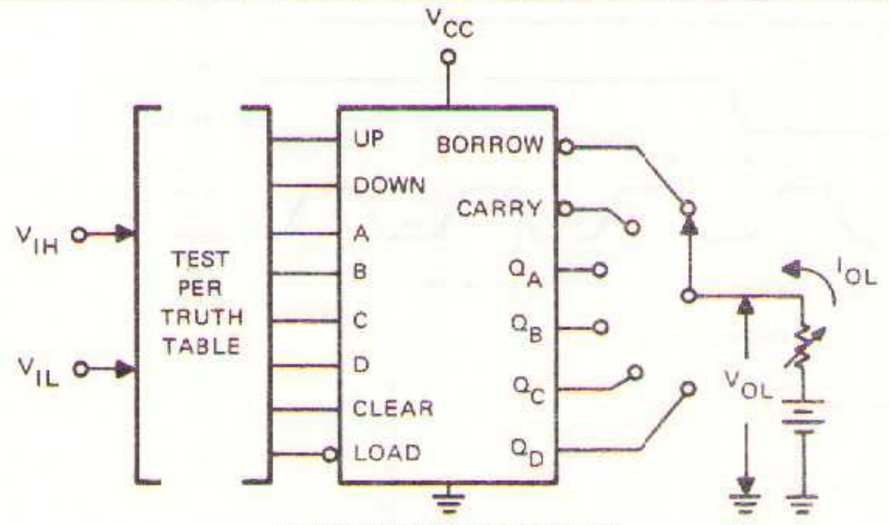
functional block diagram





Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

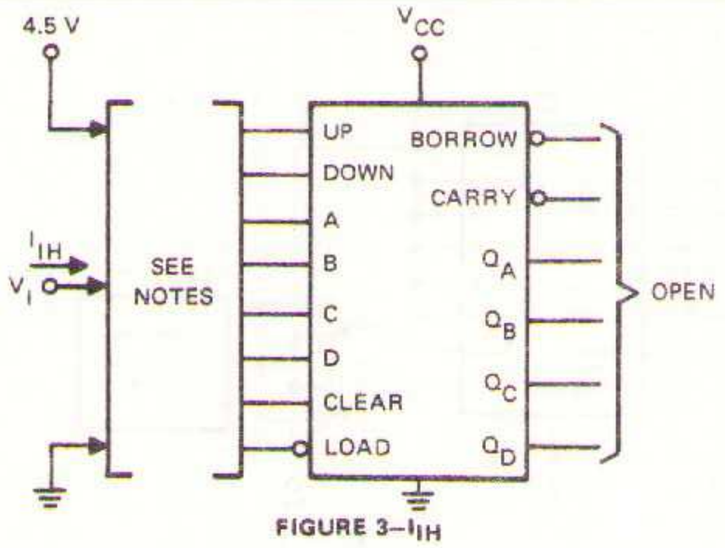
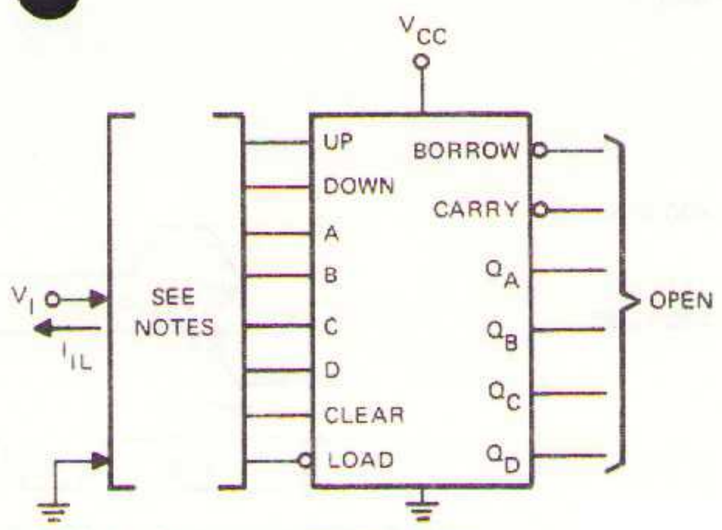
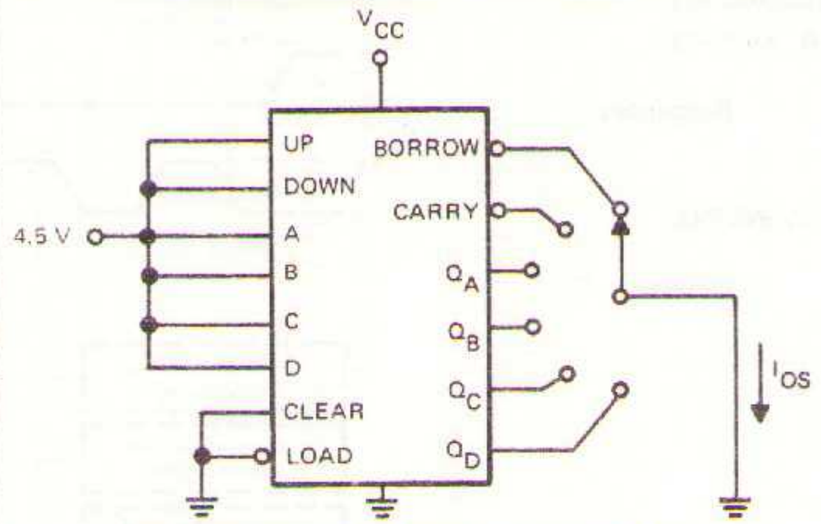


FIGURE 3–I_{IH}



NOTES: A. Each input is tested separately.
B. Apply V_I to input under test and ground other inputs.

FIGURE 4–I_{IL}



Each output is tested separately in the high-level state.

FIGURE 5–I_{OS}

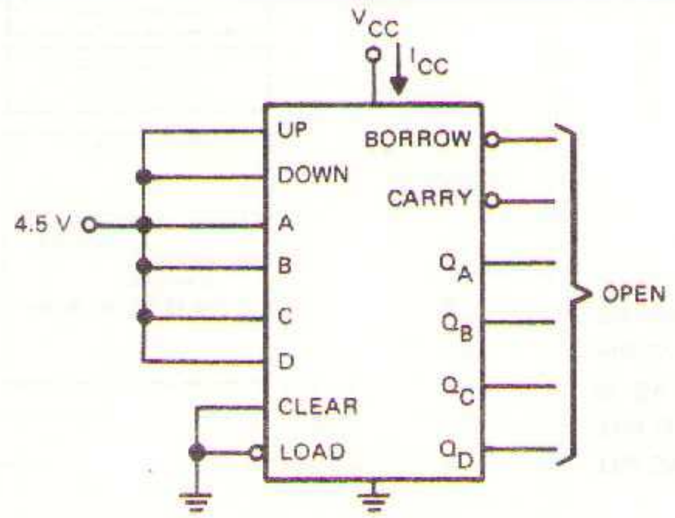


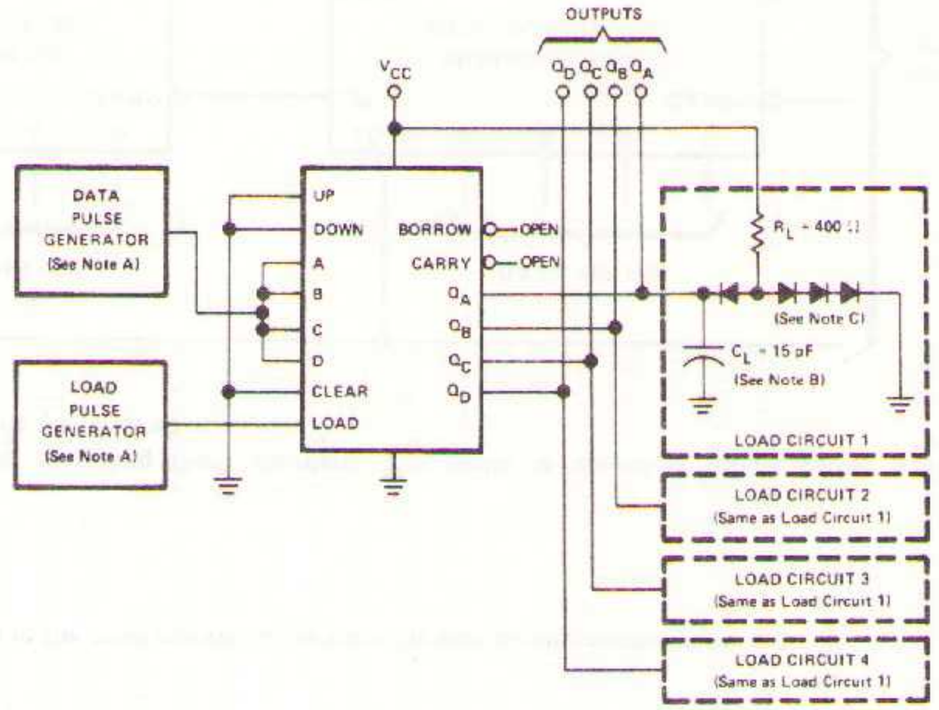
FIGURE 6–I_{CC}

NOTES: A. Each input is tested separately.
B. Apply V_I to input under test, and ground other inputs except when testing data inputs, apply 4.5 V to clear and load inputs.

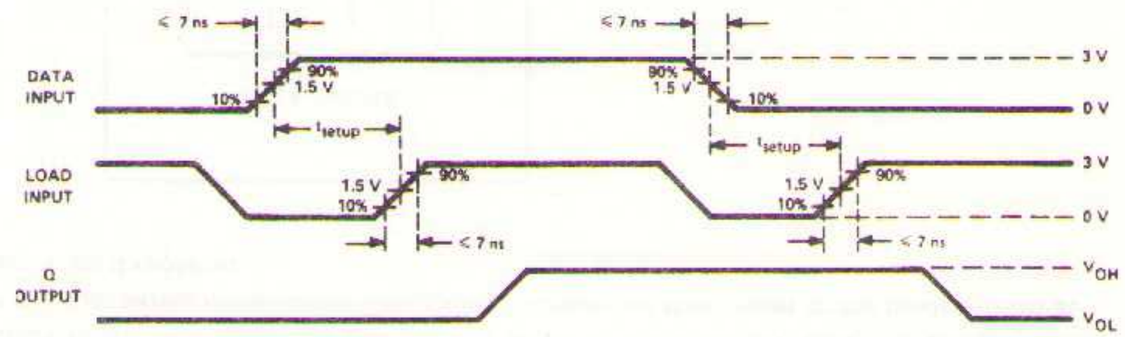
¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



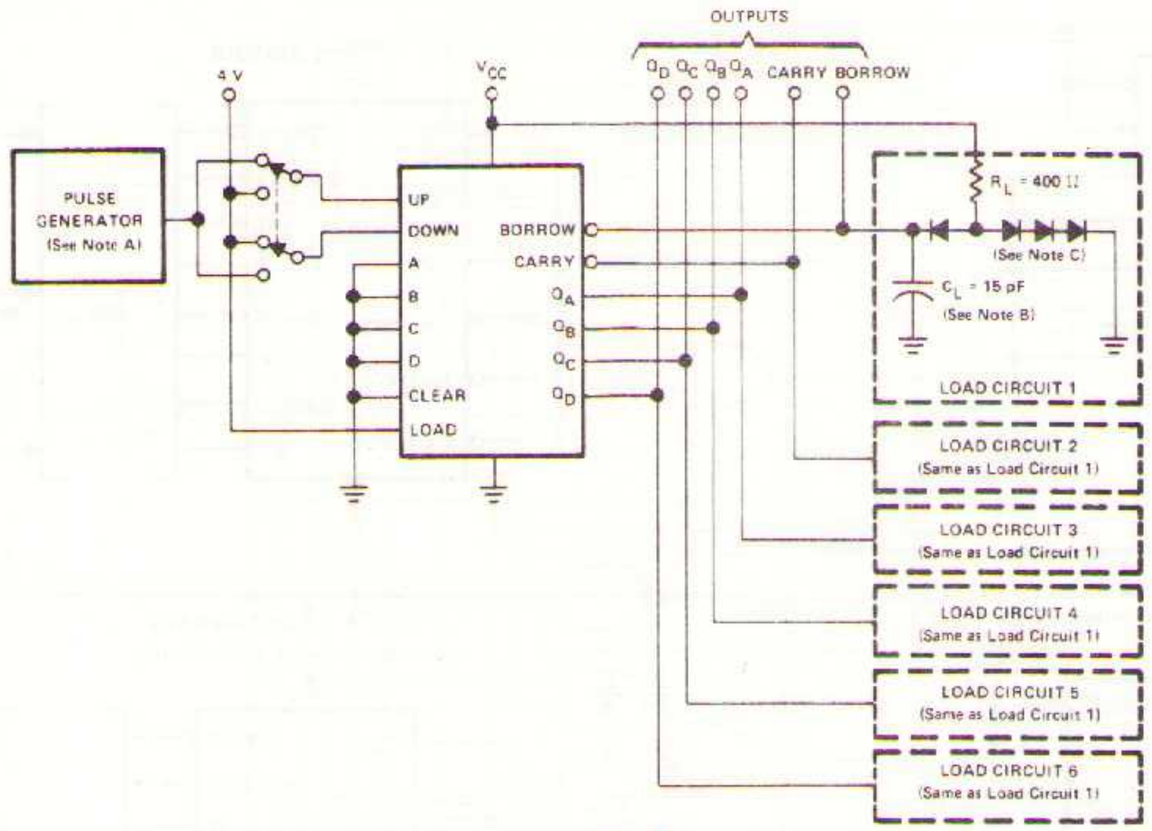
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for the data pulse generator, PRR = 500 kHz, duty cycle = 50%; for the load pulse generator, PRR = 1 MHz, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

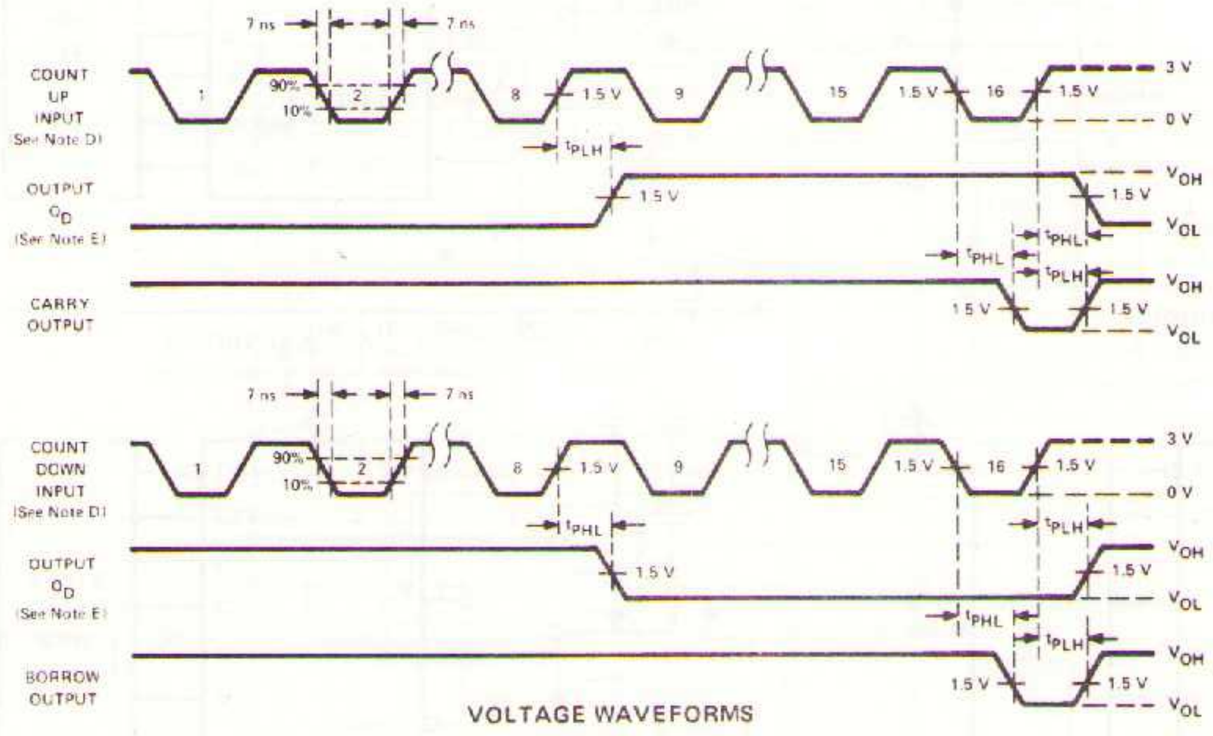
FIGURE 7–SETUP TIME

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

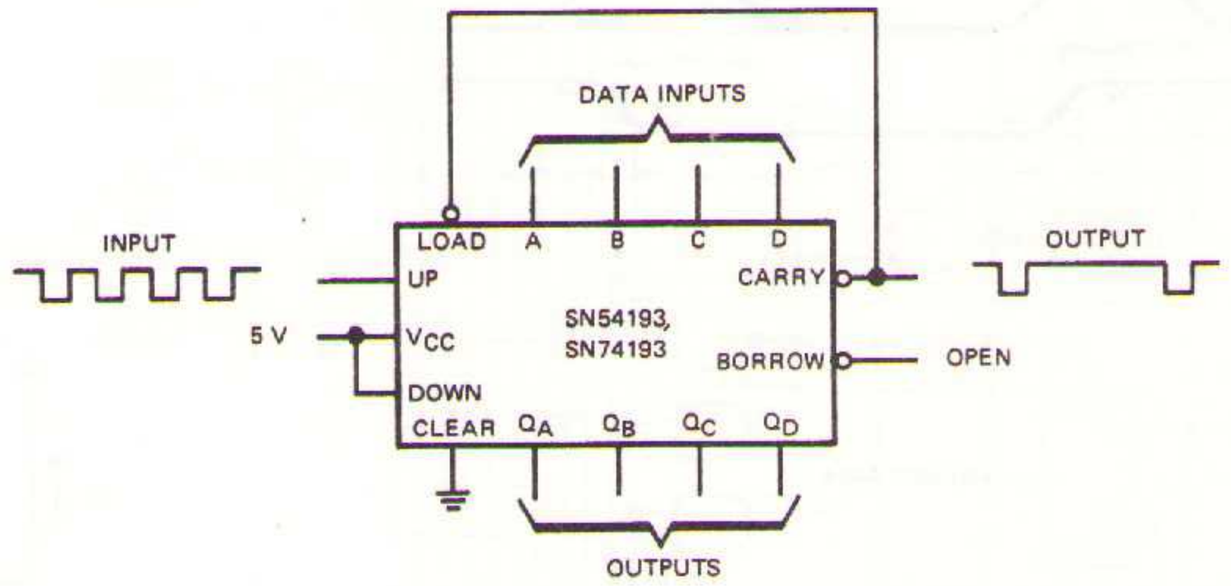
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Count-up and count-down pulses shown are for the SN54193/SN74193 binary counters. Count cycle for SN54192 decade counter is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.

FIGURE 8—PROPAGATION DELAY TIMES

TYPICAL APPLICATION DATA

modulo-N divider

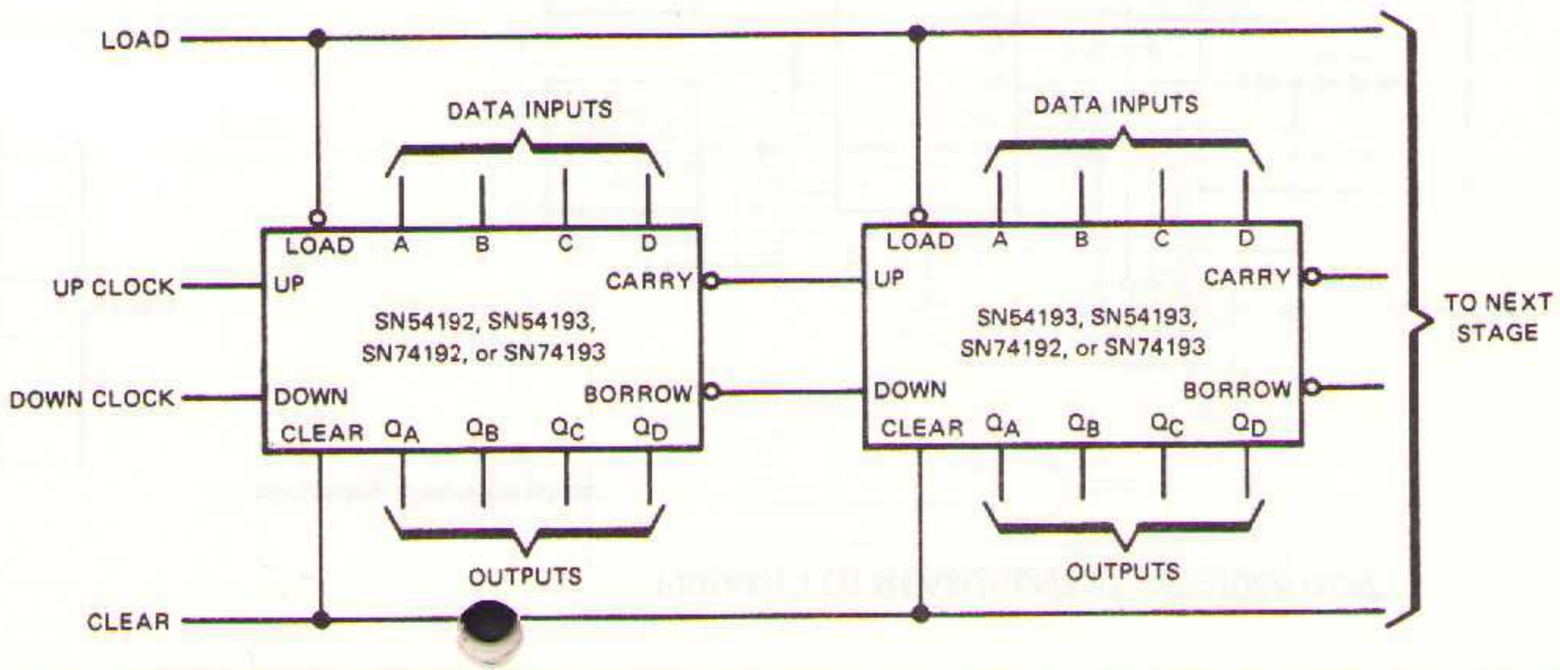
The SN54193/SN74193 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. By connecting the carry output to the load input, the counter will count to the maximum state (15) and the data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated.



The SN54192/SN74192 may be used in the same manner to perform division by any number from 1 to 10.

cascading

Circuitry is provided internally for cascading these counters. The mode of cascading shown below is ripple borrow/carry. No external components are required.



Overzicht van publicaties van technische gegevens TTL serie.

typenummer	deel	pag.	omschrijving
SN 7400N	5/6	20	Quadruple 2-input positive NAND gate.
SN 7402N	5/6	20	Quadruple 2-input positive NOR gate.
SN 7404N	5/6	21	Hex inverter.
SN 7406N	11/12	4	Hex inverter buffer/driver (30 volt).
SN 7408N	11/12	6	Quadruple 2-input positive AND gate.
SN 7409N	11/12	6	Quadruple 2-input positive AND gate.
SN 7410N	5/6	21	Triple 3-input positive NAND gate.
SN 7413N	5/6	22	Dual Schmitt trigger.
SN 7416N	11/12	4	Hex inverter buffer/driver (15 volt).
SN 7420N	5/6	22	Dual 4-input positive NAND gate.
SN 7426N	11/12	8	Quadruple 2-input positive NAND gate (15 volt)
SN 7430N	5/6	23	8-input positive NAND gate.
SN 7440N	5/6	23	Dual 4-input positive NAND buffer.
SN 7441AN	5/6	24	Decoder/nixie driver (zie verder: SN 74141AN).
SN 7442N	5/6	26	BCD - to - Decimal decoder.
SN 7446N	11/12	10	BCD-to-Seven segment decoder/driver (20 mA sink).
SN 7447N	11/12	10	BCD-to-Seven segment decoder/driver (20 mA sink).
SN 7448N	11/12	10	BCD-to-Seven segment decoder/driver (10 mA sink).
SN 7450N	5/6	29	Expandable dual 2-wide 2-input AND-OR-INVERT gate.
SN 7451N	5/6	29	Dual 2-wide 2-input AND-OR-INVERT gate.
SN 7453N	5/6	30	Expandable 4-wide 2-input AND-OR-INVERT gate.
SN 7454N	5/6	30	4-wide 2-input AND-OR-INVERT gate.
SN 7460N	5/6	31	Dual 4-input expander.
SN 7470N	5/6	31	J-K flip-flop.
SN 7472N	5/6	33	J-K master-slave flip-flop.
SN 7473N	5/6	34	Dual J-K master-slave flip-flop.
SN 7474N	5/6	36	Dual D-type edge-triggered flip-flop.
SN 7475N	5/6	38	Quadruple bistable latch.
SN 7476N	5/6	42	Dual J-K master-slave flip-flop with preset and clear.
SN 7480N	5/6	43	Gated full adder.
SN 7482N	11/12	20	2-bit binary full adder.
SN 7483N	11/12	24	4-bit binary full adder.
SN 7486N	5/6	48	Quadruple 2-input exclusive OR gate.
SN 7490N	5/6	50	Decade counter.
SN 7491AN	11/12	28	8-bit shift register.
SN 7492N	5/6	52	Divide-by-twelve counter.
SN 7493N	5/6	55	4-bit binary counter.
SN 7494N	11/12	30	4-bit shift register.
SN 7495N	11/12	32	4-bit right-left shift register.
SN 7496N	11/12	36	5-bit shift register.
SN 74100N	5/6	38	Dual quadruple bistable latches.
SN 74107N	5/6	34	Dual J-K master-slave flip-flop (as SN 7473N).
SN 74121N	5/6	58	Monostable multivibrator.
SN 74141AN	11/12	38	BCD-to-decimal decoder/driver (nixie-tube).
SN 74150N	11/12	41	16-bits data selector.
SN 74151N	11/12	41	8-bits data selector (with strobe).
SN 74153N	11/12	47	Dual 4-line-to-1-line data selector/multiplexer.
SN 74155N	11/12	51	Dual 2-to-4-line decoder/demultiplexer.
SN 74156N	11/12	51	Dual 2-to-4-line decoder/demultiplexer (open collector).
SN 74180N	11/12	55	8-bit odd/even parity generator/checker.
SN 74192N	11/12	58	Synchroon decade up/down counter.
SN 74193N	11/12	58	Synchroon 4-bits up/down counter.

Van de overige in ons leveringsprogramma opgenomen TTL IC's worden in 1971 de gegevens nog gepubliceerd; via ons hoofdkantoor te Rotterdam kunnen op aanvraag fotokopieën verstrekt worden à ƒ 0,40 per A-4 pagina +14% B.T.W. Deze kopieën worden U bij betaling met een gegarandeerde postcheque of betaalcheque franco toegezonden. Voor prijzen van deze en andere IC's verwijzen wij U naar onze prijslijst, welke U op aanvraag ook kan worden toegezonden voor zover deze nog niet in Uw bezit mocht zijn.

DAM ELEKTRONICA - VAN DAM ELEKTRONICA - VAN DAM ELEKTRONIC

440 VERSCHILLENDE VOORRAADTYPEN HALFGELEIDERS

ATTENTIE: Onderstaande stuksprijzen zijn exclusief 14 % BTW; industrieprijzen op aanvraag.

Germanium transistoren

AC125	ƒ 1,33 s
AC126	1,33 s
AC127	1,33 s
AC127/128	2,75 s
AC132	1,33 s
AC187/188	2,86 s
AC187/188K	3,26 s
AD139	4,27 s
AD149	3,47 s
AD161/162	6,02 s
AF118	2,13 s
AF121	2,09 s
AF124	1,73 s
AF125	1,63 s
AF126	1,43 s
AF127	1,43 s
AF239	3,06 s
ASY27	2,91 s
ASZ18	6,38 s
2N456A	7,40 s
2N1304	1,40 s
2N1305	1,40 s

Silicium transistoren

2C415	7,44
2N706	1,25 s
2N708	1,23 s
2N914	1,58 s
2N1613	1,76 s
2N1711	1,76 s
2N1893	1,80 s
2N2102	2,31 s
2N2219A	1,89 s
2N2222A	1,73 s
2N2904A	1,98 s
2N2905A	1,98 s
2N2907A	1,87 s
2N3011	1,23 s
2N3012	2,04 s
2N3053	3,30 s
2N3054	5,30 s
2N3055USA !	6,50 s
2N3375	35,21 s
2N3553	13,26 s
2N3632	45,90 s
2N3702	1,21 s
2N3704	1,05 s
2N3707	1,14 s
2N3708	1,00 s
2N3711	1,07 s
2N3713	15,70 s
2N3789	23,50 s
2N3866	11,07 s
2N3904	2,80
2N3906	2,80
2N4036	6,00 s
2N4347	14,35 s
2N4905	17,00 s
2N4914	11,90 s
2N5034	6,05 s
2N5036	6,45 s
2N5320	8,00
2N5322	9,15
2N5323	6,45 s
BC107B	1,27 s
BC108B	1,33 s
BC109C	1,33 s
BC121	2,24
BC135	1,66 s
BC136/137	3,96 s
2 x BC138	4,96 s
BC147B	1,22 s
BC148B	1,17 s
BC149C	1,33 s
BC154	1,98 s
BC159B	1,33 s
BC170B	0,80 s
BC171B	0,90 s
BC177	1,68 s
BC178B	1,58 s
BC179B	1,68 s
BC181A	1,04 s
BC182B	0,88 s
BC183B	0,88 s
BC184B	1,01 s
BC184C	1,07 s
BC212B	1,25 s
BC213B	1,07 s
BC214B	1,24 s
BD107B	9,45
BD115	4,28 s
BD124	5,66 s
BF118	5,49
BF123	2,48
BF125	2,48
BF127	2,34
BF125	2,05 s
BF165	2,20 s
BF166	2,75 s
BF167	2,42 s
BF194	1,48 s
BF195	1,48 s
BF224	1,17 s
BF259	4,50 s
BF298	2,70 s
BF357	4,30 s
BFX41	4,21
BFY56A	2,53
BFY64	1,85 s
BFY72	2,49 s
BFY90	11,00 s
C407	1,43 s
MD7001	9,00
MJE340	5,62
MJE370	5,40
MJE371	5,85
MPSA-12	4,05
TIP29	3,63 s
TIP29A	4,00 s
TIP30	4,30 s
TIP30A	4,68 s
TIP31	4,51 s
TIP32	5,18 s
TIP33A	7,48 s
TIP34A	10,90 s
TIP35A	20,57 s
TIP36A	27,50 s
TIS60	1,36 s
TIS61	1,62 s
TIS62	1,75 s
TIS97	1,73 s
40233	3,10 s
40316	4,50 s
40317	3,80 s
40360	4,35 s
40361	4,90 s
40362	5,95 s
40363	8,75 s
40406	5,65 s
40407	3,90 s
40408	5,20 s
40409	5,55 s
40410	6,35 s
40411	20,65 s
40594	10,70 s
40595	10,70 s

FET transistoren

2N3819	2,30 s
2N3820	3,84
2N3823	10,40
2N4857	13,60
2N5245	3,50 s
3N128	7,05 s
3N140	7,85 s
3N141	7,50 s
40673	10,00 s
BF245B	2,40 s
BF247B	3,00 s
TA7153	15,35 s
TAA320	3,05 s
TIS34	2,36 s
SU2099A	22,50 s

Uni-junction transistoren

2N2646	4,59
2N2647	14,85
2N4893	3,90 s
D13T1	4,72
TIS43	2,36

Tunneldioden

TD716	4,27

Varicap dioden

BA102	1,43 s
BA110	1,85
BA141	4,80
BA142	3,05
BA163	8,10

Geïntegreerde schakelingen, lineair

CA3000	18,25 s
CA3012	8,75 s
CA3018	7,85 s
CA3020	12,40 s
CA3028	7,00 s
CA3035	11,90 s
CA3046	7,85 s
CA3048	19,45 s
CA3059	15,55 s
CA3062	23,50 s
PA230	13,50 s
PA237	17,10 s
PA246	24,75 s
MC1429G	14,75 s
MC1430P	15,00 s
MC1435P	27,00 s
MC1439G	9,50 s
MC1460G	15,25 s
L005T1	12,50 s
L036T1	12,50 s
L037T1	12,50 s
LM703L	3,85 s
RC703T	4,50 s
µA723C	8,95 s
SAJ110	24,10 s
SN72702L	5,25 s
SN72702N	4,80 s
SN72709DN	5,55 s
SN72709L	3,35 s
SN72709N	3,00 s
SN72710L	4,80 s
SN72710N	4,40 s
SN72711L	3,95 s
SN72711N	3,65 s
SN72741L	4,10 s
SN72741N	3,75 s
SN72741P	5,05 s
SN75451P	6,80 s
TAA263	5,80 s
TAA293	6,05 s
TAA310	6,35 s
TAA710	10,80 s

Geïntegreerde schakelingen, digitaal, RTL

MC717P	7,19 s
MC718P	6,30 s
MC719P	7,20 s
MC767P	25,20 s
MC780P	25,20 s
MC788P	7,65 s
MC789P	7,20 s
MC790P	10,80 s
MC792P	7,20 s
µL914	3,70 s
µL923	6,75 s

Geïntegreerde schakelingen, digitaal, TTL

Onderstaande prijzen gelden bij afname van 1-24 IC's in één koop. Bij aanschaf van 25-99 stuks (dezelfde of verschillende typen) dienen deze prijzen met 0,76923 te worden vermenigvuldigd.

type	1-24
SN7400N	2,76 s
SN7401N	2,76 s
SN7402N	2,76 s
SN7403N	2,81 s
SN7404N	3,07 s
SN7405N	3,22 s
SN7406N	6,19 s
SN7407N	6,19 s
SN7408N	3,26 s
SN7409N	3,26 s
SN7410N	2,76 s
SN7413N	6,15 s
SN7416N	4,85 s
SN7417N	4,85 s
SN7420N	2,76 s
SN7423N	3,69 s
SN7425N	3,35 s
SN7426N	3,38 s
SN7427N	3,78 s
SN7428N	4,63 s
SN7430N	2,76 s
SN7432N	3,84 s
SN7437N	4,63 s
SN7438N	4,63 s
SN7440N	3,07 s
SN7441AN	12,19 s
SN7442N	11,66 s
SN7443N	13,90 s
SN7444N	13,90 s
SN7445N	21,81 s
SN7446N	22,71 s
SN7447N	19,68 s
SN7448N	13,90 s
SN7450N	2,81 s
SN7451N	2,81 s
SN7453N	2,81 s
SN7454N	2,81 s
SN7460N	2,81 s
SN7470N	4,68 s
SN7472N	3,47 s
SN7473N	5,56 s
SN7474N	4,94 s
SN7475N	7,97 s
SN7476N	5,97 s
SN7480N	7,09 s
SN7481N	11,22 s
SN7482N	9,04 s
SN7483N	14,52 s
SN7484N	11,75 s
SN7485N	31,62 s
SN7486N	3,38 s
SN7490N	8,37 s
SN7491AN	12,82 s
SN7492N	8,81 s
SN7493N	8,37 s
SN7494N	11,75 s
SN7495N	9,09 s
SN7496N	14,78 s
SN7497N	49,87 s
SN74100N	31,62 s
SN74104N	8,10 s
SN74105N	8,10 s
SN74107N	5,56 s
SN74110N	8,10 s
SN74111N	17,90 s
SN74121N	6,59 s
SN74122N	8,32 s
SN74123N	18,71 s
SN74141AN	12,19 s
SN74145N	21,02 s
SN74150N	36,60 s
SN74151N	14,60 s
SN74153N	13,36 s
SN74154N	31,34 s
SN74155N	14,43 s
SN74156N	13,90 s
SN74160N	59,22 s
SN74161N	59,22 s
SN74162N	59,22 s
SN74163N	59,22 s
SN74164N	34,55 s
SN74165N	37,84 s
SN74166N	36,96 s
SN74170N	27,34 s
SN74180N	17,81 s
SN74181N	80,59 s
SN74182N	17,90 s
SN74184N	64,56 s
SN74185N	64,56 s
SN74190N	28,85 s
SN74191N	28,85 s
SN74192N	30,63 s
SN74193N	30,63 s
SN74194N	31,17 s
SN74195N	31,17 s
SN74196N	23,06 s
SN74197N	23,06 s
SN74198N	50,77 s
SN74199N	50,77 s

Fotodioden

APY12	4,50 s
OAP12	8,15 s

LED's (licht emitterende dioden)

TIL201	13,50 s
TIL202	9,10 s

Silicium dioden

1N914	0,38 s
1N3754	1,55 s
1N4143	2,79 s
1N4148	0,38 s
1N4448	0,49 s
1N5060	1,20 s
12F5	5,05 s
21PT10	4,25 s
41HF5	5,90 s
41HFR5	5,90 s
BA130	0,60 s
BY133	1,35 s
BYY33	1,35 s
EKS1/02	0,86 s
ESK1/06	0,90 s
ESK1/10	0,99 s
ESK1/12	1,05 s

Germanium dioden

AA134	0,27 s
SFD107	0,27 s

ITT/SIEMENS/ SEMOKRON

Bruggelijkrichters, silicium, printmodel

B40C400	2,25
B40C800	2,40
B40C1200	2,61
B40C2200/3300	3,57
B40C3300/5000	8,10
B80C400	2,40
B80C2200/3300	5,51
B80C3300/5000	8,10
B250C2200/3300	7,20
B500C2200/3300	11,25

ITT en/of TI

Zenerdioden
400 mW

ZG 2,7	
ZG 3,3 / 1N746A	
1N747A (3,6 V)	
ZG 3,9 / 1N748A	
1N749A (4,3 V)	
ZG 4,7 / 1N750A	
1N751A (5,1 V)	
ZG 5,6 / 1N752A	
1N753A (6,2 V)	
ZG 6,8 / 1N754A	
1N755A (7,5 V)	
ZG 8,2 / 1N756A	
1N757A (9,1 V)	
ZG 10 /1N758A	
ZG 12 /1N759A	
ZG 15	ZG 18
ZG 22	ZG 27
ZG 33	
Stuksprijs	ƒ 1,56 s

ITT

Zenerdioden
1.000 mW

ZD 3,9	ZD 4,3
Stuksprijs	ƒ 2,94 s
ZD 4,7	ZD 11
ZD 5,1	ZD 12
ZD 5,6	ZD 13
ZD 6,2	ZD 15
ZD 6,8	ZD 16
ZD 7,5	ZD 18
ZD 8,2	ZD 20
ZD 9,1	ZD 22
ZD 10	
Stuksprijs	ƒ 2,52 s
ZD 24	ZD 51
ZD 27	ZD 56
ZD 30	ZD 62
ZD 33	ZD 68
ZD 36	ZD 75
ZD 39	ZD 82
ZD 43	ZD 91
ZD 47	
Stuksprijs	ƒ 3,00 s
ZD 100	ZD 150
ZD 110	ZD 160
ZD 120	ZD 180
ZD 130	ZD 200
Stuksprijs	ƒ 3,78 s

Thyristoren

2N4172	14,20
2N4441	4,77 s
2N4442	7,15 s
2N4443	9,95 s
2N4444	16,75 s
3N83 (BRY39)	
3N84	6,30
BRY39 (3N84)	2,55 s
11T4	4,95 s
12T4	5,25 s
MCR2305/6	14,20
IRC10	3,15 s
TIC46	3,60 s
TIC47	4,60 s

Triacs

SC50D	30,00
TIC222D	13,50 s
TIC231D	20,00 s
40430	13,05 s
40576	15,75 s
40669	10,50 s

Triggerdioden (diacs)

1N5411	2,95 s
TIC56	1,95 s

Bovenstaande prijzen zijn exclusief 14 % BTW. Postorders en correspondentie uitsluitend richten aan: NV Technische Handelmaatschappij Van Dam Elektronica, Afdeling: verkoop, Postbus 3149 te Rotterdam-noord, Holland.

NV TECHNISCHE HANDELSMAATSCHAPPIJ

van dam
ELEKTRONICA

Hoofdkantoor: Snellemanstraat 10, Rotterdam. Tel.: 010 - 24 55 16

Verkoop: Snellemanstraat 11, Postbus 3149, Rotterdam-noord. Tel.: 010 - 24 08 12 - 24 34 97, Postgirorekening: 295550. Bankrelatie: Amsterdam-Rotterdam bank, Middellandstraat, Rotterdam.

Verkooppunt Amsterdam: Blasiusstraat 14-16, tel.: 020 - 94 72 18.

maart 1971